NASA CR-174711
UTRC-R83-925312-25

NASA

HIGH-TEMPERATURE OPTICALLY ACTIVATED GaAs POWER SWITCHING FOR AIRCRAFT DIGITAL ELECTRONIC CONTROL

by J.M. Berak, D.H. Grantham, J.L. Swindal,
J.F. Black, and L.B. Allen

UNITED TECHNOLOGIES CORPORATION
United Technologies Research Center

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
NASA Lewis Research Center

Contract NAS3-22535

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA CR-174711		

4. Title and Subtitle	5. Report Date
High-Temperature Optically Activated GaAs Power Switching for Aircraft Digital Electronic Control	May 1983
	6. Performing Organization Code

7. Author(s)	8. Performing Organization Report No.
J. M. Berak, D. H. Grantham, J. L. Swindal, J. F. Black and L. B. Allen	UTRC R83-925312-25
	10. Work Unit No.

9. Performing Organization Name and Address	11. Contract or Grant No.
United Technologies Corporation United Technologies Research Center East Hartford, Connecticut 06108	NAS3-22535
	13. Type of Report and Period Covered

12. Sponsoring Agency Name and Address	13. Type of Report and Period Covered
National Aeronautics and Space Administration Lewis Research Center Cleveland, Ohio 44135	Contractor Report
	14. Sponsoring Agency Code

15. Supplementary Notes

Project Manager, Mr. Robert Baumbick
NASA Lewis Research Center
Cleveland, Ohio 44135

16. Abstract

Gallium arsenide high-temperature devices were fabricated and assembled into an optically activated pulse-width-modulated power control for a torque motor typical of the kinds used in jet-engine actuators. A bipolar heterojunction phototransistor with gallium aluminum arsenide emitter/window, a gallium arsenide junction field-effect power transistor and a gallium arsenide transient-protection diode were designed and fabricated. A high-temperature fiber optic/phototransistor coupling scheme was implemented. The devices assembled into the demonstrator were successfully tested at 250°C, proving the feasibility of actuator-located switching of control power using optical signals transmitted by fibers.

Assessments of the efficiency and technical merits were made for extension of this high-temperature technology to local conversion of optical power to electrical power and its control at levels useful for driving actuators. Optical power sources included in the comparisons were an infrared light-emitting diode, an injection laser diode, tungsten-halogen lamps and arc lamps. Optical-to-electrical power conversion was limited to photovoltaics located at the actuator. Impedance matching of the photovoltaic array to the load was considered over the full temperature range, -55°C to 260°C. Loss of photovoltaic efficiency at higher temperatures was taken into account. Serious losses in efficiency are (1) in the optical source and the cooling which they may require in the assumed 125°C ambient, (2) in the decreased conversion efficiency of the gallium arsenide photovoltaic at 260°C, and (3) in impedance matching. Practical systems require improvements in these areas.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
High-temperature Devices, Optically Activated Switch, Gallium Arsenide Devices, Fiber Optics, Digital Electronic Control, Fly-by-Light, Gallium Arsenide Phototransistor, Power-by-Light, Gallium Arsenide Junction Field-Effect Transistor	Unclassified - unlimited

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified	208	

* For sale by the National Technical Information Service, Springfield, Virginia 22161

High-Temperature Optically Activated GaAs Power Switching for Aircraft Digital Electronic Control

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF TABLES

1.0 SUMMARY

The overall objective of this program was to investigate the use of GaAs high-temperature electronic devices for pulse-width-modulated fiber optic switching of electrical power for aircraft digital electronic controls. Due to a higher semiconductor band gap, GaAs is more suited for higher-temperature application than is silicon. In addition, the incorporation of fiber optics produces favorable systems characteristics arising from high electrical resistivity and reduced weight of the transmission cabling.

In Part I of the program, GaAs devices were designed, fabricated and tested for delivery in a fly-by-light demonstration unit. These devices included a GaAlAs/GaAs phototransistor, a junction-field-effect-transistor (JFET) power switch, and a transient-protection diode for suppressing inductive voltage spikes when switching current into a torque-motor load. Optical activation of the phototransistor was accomplished by using a high-power infrared-emitting diode (IRED) with emission wavelength at 8360Å. The photoswitch devices were able to switch up to 0.1A with a 20V stand-off capability using 0.65 mW to 1.4 mW of optically coupled power at the IRED and operate at ambient temperatures between -54°C and 250°C. Extension of fly-by-light switching to higher electrical powers would be possible with higher-power GaAs JFETs or heterojunction bipolar transistors.

A feasibility study program was also conducted on power-by-light designs whereby the required torque-motor electrical power is locally generated by a photovoltaic receiving optical power from a source located at the control computer. Factors discussed that are of primary concern for high system efficiency were generation and transmission of optical power, photovoltaic power-conversion efficiency, and photovoltaic impedance matching to the load. Optical sources included in the study were a high-power injection laser diode (ILD), a high-power IRED, arc lamps, and tungsten-halogen lamps. The photovoltaic cell considered for use had a GaAlAs/GaAs ($P/p/n/n^+$) heterostructure configuration, similar to designs for concentrator solar-cell application. Calculations were made of power-conversion efficiency for maximum electrical power output from the photovoltaic between -54°C and 260°C compared to electrical power required to drive the optical sources. At 260°C system efficiencies were 2% for a matched-wavelength ILD source, 1.55% for a matched-wavelength IRED source, 1.1% for 3200°K tungsten-halogen lamp sources, and about 0.8% for Xenon short-arc lamp sources. In order for the lamps and IRED to compete with the ILD, lens focussing onto a fiber optic bundle was required. Considerations on selection of an optical source for power-by-light application were presented. A principal obstacle for achieving predicted efficiencies is impedance matching of photovoltaic to the torque-motor load. Whatever

means used to impedance match (and regulate current) must be operational between -54°C and 260°C. A scheme using single-temperature resistance matching with a GaAs photovoltaic was proposed to demonstrate power-by-light switching.

2.0 INTRODUCTION

For airborne control applications requiring a current switch, the use of optical fibers and photosensitive switches offers the benefits of increased electrical isolation from the control computer, reduced susceptibility to electromagnetic interference, reduced weight (and cost), and improved reliability. Implementation of fiber optics for engine or flight controls can be divided into two general approaches: (1) optical energy is used to control actuator power derived from another source (fly-by-light); (2) optical energy is used as the source of power for the actuator (power-by-light). As applied to torque motors, the power-by-light approach requires the use of a photovoltaic converter to provide the electrical power. A photoactivated switch is required in the fly-by-light application. In addition, the electronic devices required for advanced aircraft turbine-engine controls using fiber optics must operate at ambient temperatures as high as 260°C. Conventional silicon devices would have to be cooled for reliable operation. Specially designed silicon electronic devices can be pushed into high-temperature operation but more severe voltage limitations will accompany the increasing temperature. Also, special circuits may be required to insure operation over the full temperature range. Indeed, silicon photodevices and photovoltaics are not practical for use in fiber optic systems at high temperature due to junction leakage. The main thrust of this work was to advance the use of an alternate semiconductor, gallium arsenide, which is more suited for high-temperature application in aircraft fly-by-light and power-by-light actuator systems.

The improved high-temperature capability of GaAs arises principally from its higher energy band gap and secondarily from its higher free-electron mobility compared to silicon. The higher the semiconductor band gap, the lower is the intrinsic carrier concentration and device bulk leakage current at a particular temperature. A higher free-electron mobility means that lower internal power dissipation develops in the device. These material advantages, therefore, lead to reduction or elimination of system cooling requirements for high-temperature operation for the gallium arsenide device.

Some material properties for gallium arsenide and silicon are summarized in Table I at various temperatures (Refs. 1 and 2). The energy band gap of gallium arsenide is 0.30 eV higher than silicon at room temperature. Although this energy difference decreases to 0.25 eV at 300°C, the difference is still sufficient to result in significantly lower bulk leakage currents (dark currents in photosensitive devices) due to an exponential dependence on band-gap energy. Figure 2-1 shows reverse leakage currents as a function of

TABLE I

MATERIAL PROPERTIES OF GaAs VERSUS Si

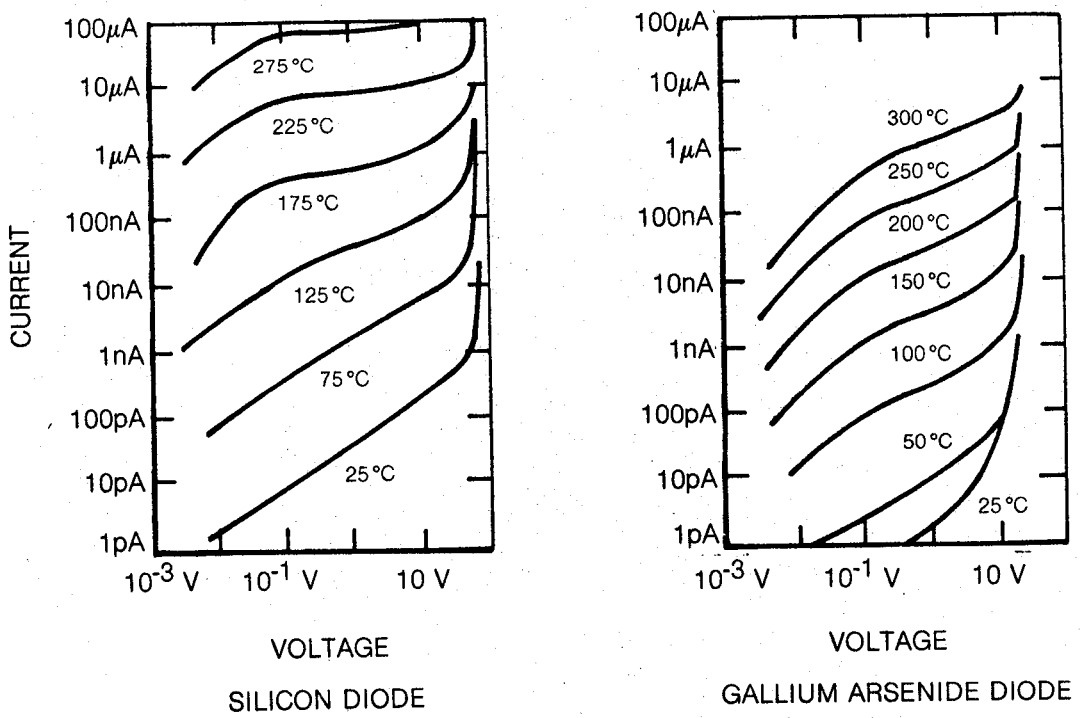
		27 °C	200 °C	300 °C
BAND GAP (ev)	Si	1.12	1.07	1.04
	GaAs	1.42	1.34	1.29
ELECTRON MOBILITY AT 1×10^{16} cm^{-3} (cm^2/V-sec)	Si	1100	360	260
	GaAs	6300	3300	3000
THERMAL CONDUCTIVITY $\left(\frac{WATT}{cm\ °C}\right)$	Si	1.43	0.86	0.65
	GaAs	0.44	0.28*	0.23*
PHOTOVOLTAIC OUTPUT, V_{mp} (VOLTS)	Si	0.47	0.12	< 0.05 (260 °C)
	GaAs	0.86	0.55	0.37

* - ESTIMATED (REF . 1)

FIG. 2-1

REVERSE CURRENT-VOLTAGE CHARACTERISTICS AT VARIOUS TEMPERATURES

REF. 3



83–3–119–1

voltage at various temperatures for gallium arsenide and silicon diodes (Ref. 3). If leakage currents are compared, then a 75-100°C operating temperature advantage will be obtained using the gallium arsenide device compared to its silicon counterpart. Alternatively, the silicon device will develop about two orders of magnitude more bulk leakage current at higher operating temperatures. Dark currents and noise in silicon photodetectors limit their use to under 150-200°C. Resulting maximum-power voltage output (V_{mp}) for a silicon photovoltaic is also too low for practical use (less than 50 mV at 260°C). GaAs photodevices and photovoltaics will operate well in the 260°C to 300°C temperature range.

The free-electron mobility in gallium arsenide is significantly greater than for silicon over the entire temperature range. A six-fold mobility advantage for GaAs at room temperature increases to a factor of 11 at 300°C. Partially offsetting this advantage of gallium arsenide for power devices is the fact that the thermal conductivity of silicon is about a factor of three higher over the full temperature range. However, if one defines a figure of merit for device temperature rise that is proportional to electron mobility multiplied by thermal conductivity, an overall advantage still rests with gallium arsenide.

The subject program was divided into two parts: (I) a hardware fly-by-light development effort and (II) a follow-on study program on power-by-light and fly-by-light designs. The objective of Part I was to design, fabricate and test a high-temperature photodetector which was compatible with pulsewidth modulation for aircraft digital electronic control and could operate a switch to provide power for a torque-motor load. The photoswitch system had to be capable of operation at ambient temperatures of -54°C to 250°C and be able to switch up to 100 mA of current with an off-state voltage of +20V. This part of the program terminated with delivery of a breadboard for demonstration of fiber optic switching using high-temperature GaAs devices. The objective of Part II was to conduct a feasibility study on designs to utilize optical energy to operate an actuator at up to 260°C. Emphasis was on power-by-light design using a GaAs photovoltaic cell to supply torque-motor power. Improvements on the original fly-by-light design of Part I were also studied. The study effort concluded with recommendations for configurations for future hardware development. This report is divided into two parts which describe the respective work performed.

PART I

DESIGN, FABRICATION AND TESTING OF A HIGH-TEMPERATURE PHOTOSWITCH SYSTEM

3.0 PHOTOSWITCH SYSTEM DESIGN

System design for the fly-by-light breadboard demonstrator was divided into two parts -- (1) design of the required GaAs high-temperature devices and (2) design of the optical path. In the first part, consideration was given to selection of devices and their design to meet the program goals. During this part of the program electrical measurements at high temperature on existing GaAs phototransistors were required in order to properly design the optical switch system and assure validity of the design concept. The question of supplying optical energy to the photosensitive device was addressed in the design of the optical path. Here, important factors were selection of source, coupling of source to optical fiber, fiber transmission and connector loss, and optical coupling to the photosensitive device. The delivered hardware was designed to permit high-temperature testing of the GaAs devices. The other breadboard components, e.g., power supplies and optical source, were not to be subjected to the high-temperature environments. A description of the breadboard is given in Appendix I.

3.1 GaAs Devices and Circuit

Specific design goals for the photoswitch devices included: (1) operation for up to two hours at 250°C; (2) operation at temperatures as low as -54°C; (3) 100-mA switching capability with an off-state voltage of +20V; and (4) compatibility with pulse-width modulation for turbine-engine electronic control using torque motors. GaAs-based semiconductor devices were chosen over silicon for high-temperature application, principally due to the higher GaAs energy band gap.

The ideal photoswitch would be one that has both optical sensitivity and power handling capability; otherwise, an optically sensitive device would have to trigger another device to carry out the power switching. In implementing a control system the use of an IRED (InfraRed Emitting Diode) as optical source rather than a higher-optical-power LD (Laser Diode) is preferred due to longer lifetime, simplicity of use, and lower cost. In order to demonstrate in a conservative manner near-term fly-by-light switching in this program and be able to use the IRED optical source, the trigger approach was adopted.

At UTRC considerable experience had been gained with GaAs JFET (Junction Field-Effect Transistor) one-ampere power switches which could be used for actuator control at high environmental temperatures. The GaAs JFET device had been chosen as the power switching element because it had a low on-state resistance, could use a low-power digitially compatible gate input signal for switching, and had a p^+-n junction configuration which was stable during high-temperature operation. Individual one-ampere switches had been fabricated and operated continuously for 10,000 to 20,000 hours at 200°C with 20-30V stand-off voltage. Tests had also been conducted on lower-current JFET's (15mA level) at temperatures exceeding 300°C. Therefore, there existed a proven electrical device, which when properly scaled, could reliably switch 100 mA of current at high temperature for this program.

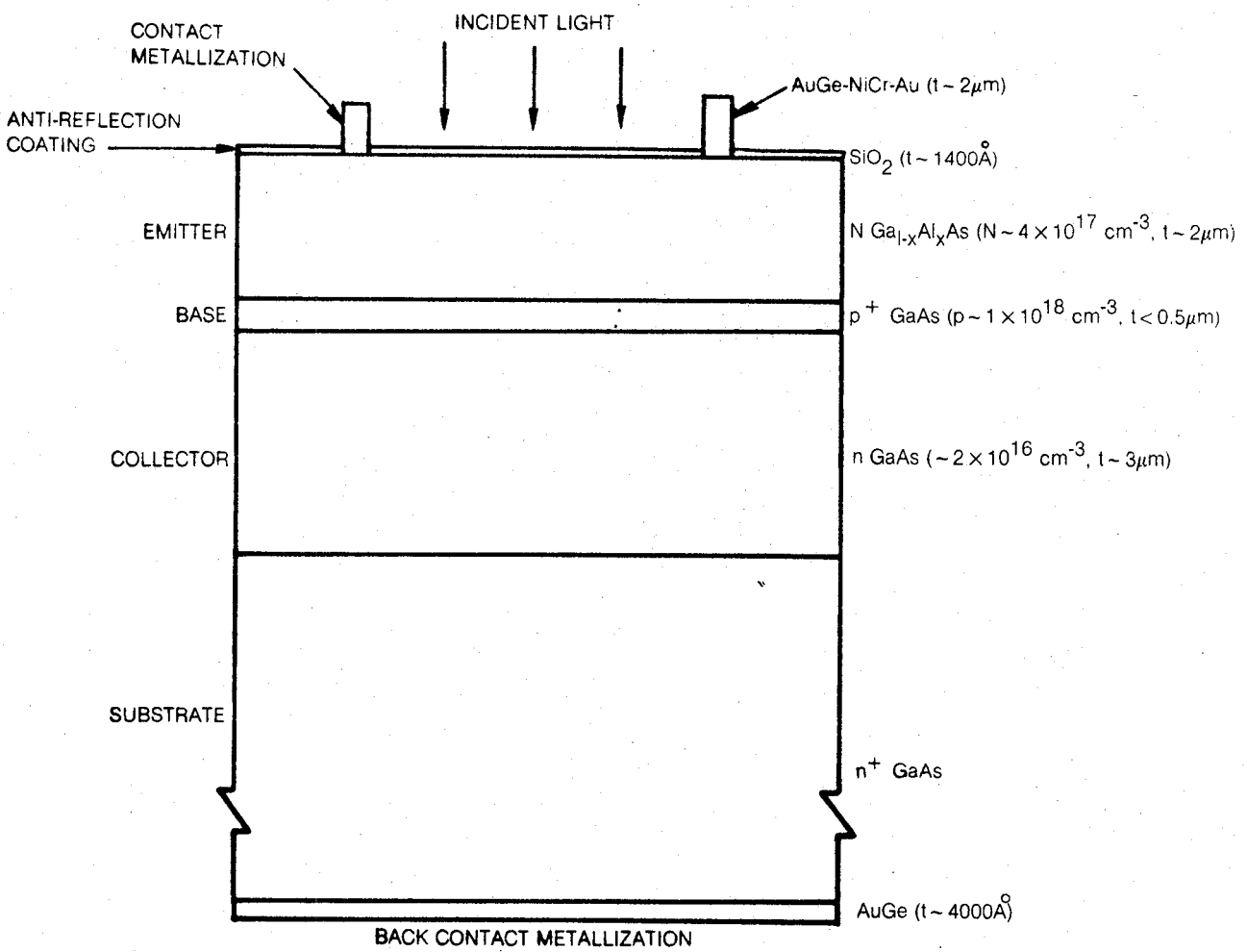
An important requirement for the photosensitive device in a fly-by-light control system is that it exhibit optical gain in order to reduce optical requirements at the IRED source. The phototransistor was chosen over other possible photodevice types because it provided gain, did not require precise biasing (as in the case of an avalanche diode), was compatible with pulse-width modulation for avionic control, and was readily fabricated using existing GaAs technology. GaAlAs/GaAs phototransistors had been fabricated at UTRC for fly-by-light application and some devices tested at up to 200-300°C with promising optical gains. For optical activation the near-infrared emission of a Group-III-V IRED source could be matched to the GaAs absorption layer of the phototransistor. The light-activated phototransistor could then be connected directly to the gate of the JFET power switch.

The GaAs devices that were designed, fabricated and tested at up to 250°C in this program therefore included: (1) a GaAlAs/GaAs phototransistor as the near-infrared photosensitive element, (2) a GaAs JFET for switching up to 100 mA into the torque-motor load, and (3) a GaAs transient-protection diode. The protection diode was placed across the torque motor and was required to eliminate high-voltage spikes which would accompany inductive load switching and which would destroy the JFET switch. The clock rate of all these devices was orders-of-magnitude faster than maximum anticipated pulse-width-modulation-control frequencies, i.e., 2 kHz.

A cross-sectional schematic diagram of the phototransistor design is shown in Fig. 3-1. This device had an $N/p^+/n$ layer structure with a surface emitter layer of $Ga_{1-x}Al_xAs$, a thin p^+-GaAs base and an n-GaAs collector. Electrical contact to the phototransistor was made to the emitter through a surface metallization ring (via a bonding pad) and to the collector by way of the back surface of the substrate; the base was left floating. The device was normally off (except for dark currents) and could be switched on and exhibit optical gain when illuminated by near-infrared illumination. The ternary layer functioned as a window for the incident optical radiation and as an

FIG. 3-1

GaAlAs-GaAs PHOTOTRANSISTOR STRUCTURE



80-03-42-16

efficient electron emitter into the base. At room temperature $Ga_{1-x}Al_xAs$ can have an energy band gap between 1.43 eV and 2.1 eV, depending on the atomic fraction, x, of aluminum. As a result, this layer can pass radiation having energy below its energy gap (but above that for GaAs) to be absorbed in the GaAs base-collector layers. Since the absorption region is well below the surface of the device, surface state recombination is reduced. Optical absorption is direct in GaAs; the radiation is essentially absorbed in several microns of GaAs material. If absorption takes place in the base-collector depletion layer, the generated electron-hole pairs will be separated by the field. Outside this region, generated minority carriers must diffuse into the depletion region to contribute to a photocurrent.

The forward-biased heterojunction formed in the GaAlAs-GaAs system injects minority carriers with an almost 100% injection efficiency from the wide-gap semiconductor into the GaAs base regardless of the doping level on each side of the junction (Ref. 4). This high injection efficiency has been confirmed experimentally for an energy-gap difference of only 0.2 eV ($x = 0.15$) (Ref. 5). The possibility of electron injection through a thin GaAs base region can result in gain upon illumination. The optical gain of a phototransistor can be defined as the product of device quantum efficiency and the common-emitter current gain, β. Under conditions of 100% injection efficiency, β is given by

$$\beta = \left(\cosh\left(\frac{t_b}{L}\right) - 1\right)^{-1} \qquad (3\text{-}1)$$

where L is the diffusion length of the minority carrier and t_b is the base thickness (Ref. 5). For small values of (t_b/L), β can be approximated as $2(L/t_b)^2$. Since the electron minority current carrier has a longer lifetime in p-GaAs material then the hole minority current carrier has in n-material, a p-type GaAs base is preferred to maximize gain. For $L = 2.5$ μm (Ref. 6) and quantum efficiency = 0.8, an optical gain of 40 is expected for a device with 0.5-μm base width. Optical gains in excess of 100 have been reported for GaAlAs heterojunction phototransistors (Refs. 6 through 9). The gain has also been measured to be highly dependent upon illumination level, and this dependence has been ascribed to reduction in injection efficiency due to recombination by interface states (defect centers) at the heterojunction interface (Ref. 4). The total emitter current, I_E, of a heterojunction transistor can be written as

$$I_E = I_d + I_i \qquad (3\text{-}2)$$

where I_d is the defect current and I_i is the injected current. For low values of emitter current, the defect current at the heterojunction interface can account for a significant fraction of the total emitter current. Both the emitter efficiency, given by I_i/I_E, and the gain will therefore decrease at lower light levels if defect currents are present. The lattice match between GaAs and AlAs is quite good; the lattice constants are 5.653Å and 5.661Å, respectively (Ref. 10). However, the small lattice mismatch does produce some defects at the interface (Ref. 11). Additional defects may also be present depending on the conditions of crystal growth. In any case, defect currents will reduce injection efficiency and thus limit the gain especially under lower-level illumination.

The radiative wavelength that was utilized on the breadboard was approximately 8360Å, at which GaAs has an absorption coefficient of $10^4 cm^{-1}$ (Ref. 12). Thus, 3 μm of GaAs material (base plus collector) are sufficient to absorb 95% of the radiation passing through the ternary layer. The corresponding value of x for transparency of the $Ga_{1-x}Al_xAs$ layer is near 0.1. The acceptable range for x in this program was 0.2 to 0.4 in order to provide a safety margin during growth and also avoid excessive emitter contact resistance and layer resistance associated with an indirect-band-gap material ($x > 0.4$). Attempts were made to keep the base thickness at 0.5 μm and below. A thin quarter-wave sputtered-quartz anti-reflection coating (~ 1400Å) was also used to reduce surface reflectivity to about 5%. The question of phototransistor diameter will be addressed later in this section as well as in Section 3.2. The phototransistor measurements that were used to aid in the design studies are also included in Section 3.2.

The GaAs JFET current switch was a p^+-n device with coplanar source and drain contacts and an intervening channel region. A detailed cross-sectional view of a source-drain finger pair is shown in Fig. 3-2. The device was constructed by growing n and n^+-GaAs layers having specific carrier concentrations and thicknesses on a p^+-GaAs substrate and processing the wafer to isolate source and drain regions on the epitaxial layer side. Au-Ge contact metallization with thin nichrome and three-micron-thick gold were used to form ohmic contacts to the n^+-GaAs layer (~ $8 \times 10^{18} cm^{-3}$, t~1 μm). The p^+-GaAs substrate was the gate for the device. A feature of the structure is the etched-out channel region in the n-GaAs layer, which resulted in a channel length after etching that was typically less than 3 μm long. Under zero applied gate bias, (V_G), the built-in junction voltage (V_b) is responsible for a thin region depleted of carriers at the p^+-n junction, but current is able to flow through the undepleted material between source and drain. The depletion depth is given by

SCHEMATIC CROSS SECTION OF JFET FINGER PAIR

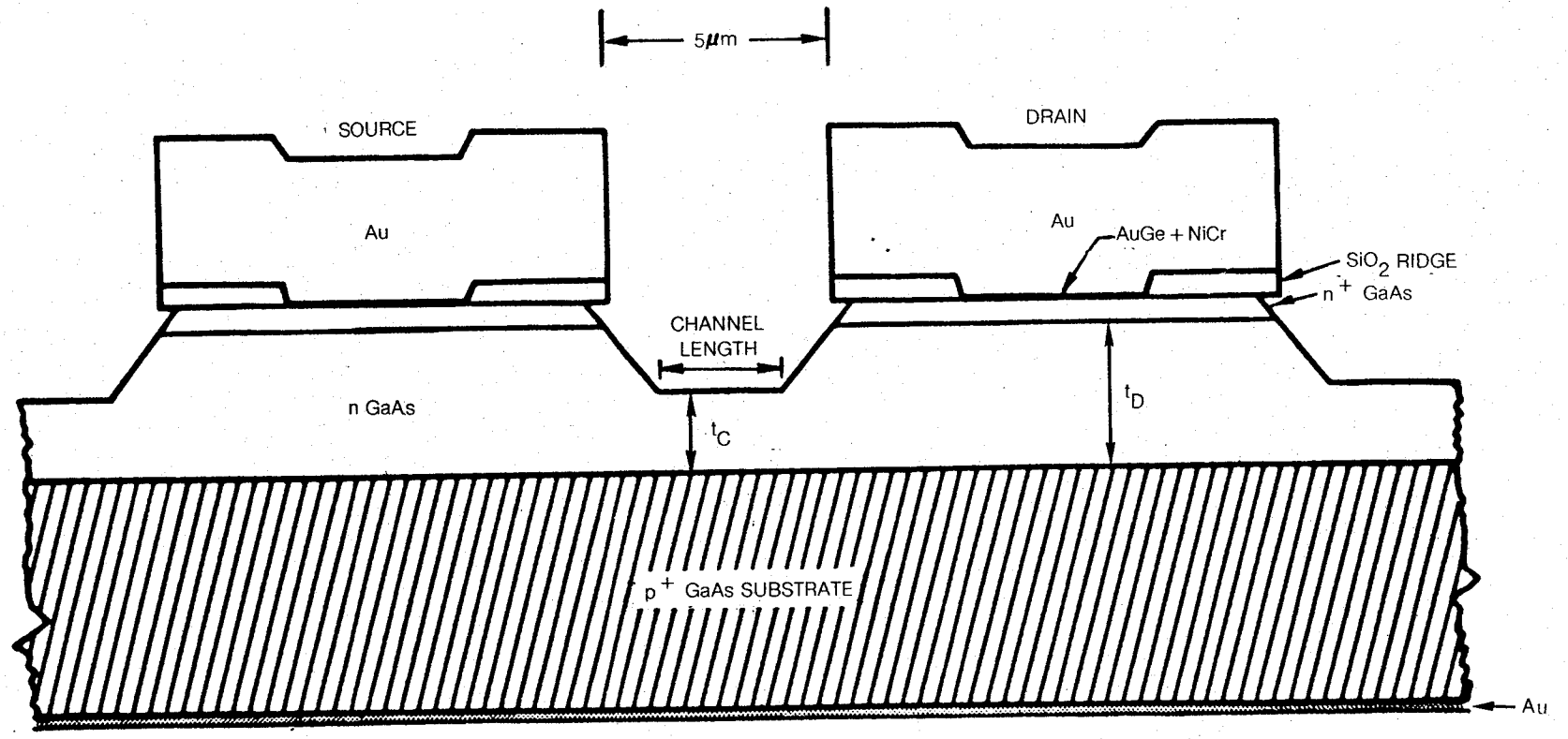


FIG. 3-2

$$t_d = \left(\frac{2K_s \varepsilon_o (-V_b - V_G)}{qn} \right)^{1/2} \qquad (3\text{-}3)$$

where K_s is the dielectric constant, ε_o is the permittivity of free space, q is the electron charge, and n is the epitaxial layer carrier concentration. Upon application of an increasingly negative gate voltage to this normally-on device, a depletion layer advances away from the junction until current is pinched off in the channel region. A pinch-off voltage, V_p, of about -12V has been in use for the JFET devices. The required epitaxial-layer thickness in the channel region for the pinch-off condition and minimum thickness underneath the drain contact can be determined with Eq. 3-3. When the device is in the off-state, the required 20V on the drain adds to the 12V on the gate and the built-in voltage, so that 33V will exist across the gate and drain. This requires an epitaxial layer with n less than $3 \times 10^{16} cm^{-3}$ in order to avoid avalanche breakdown. To allow for a margin of safety and additional voltage capability, the UTRC JFET devices had an active layer with n about $1 \times 10^{16} cm^{-3}$. For this carrier concentration a channel layer thickness (t_C) of 1.3 μm is necessary for a pinch-off voltage of -12V. Under the drain contact the GaAs epitaxial thickness (t_D) should be at least 2.1 μm in order to avoid premature breakdown.

By increasing the number of parallel source-drain finger pairs, the current carrying capacity of the JFET is increased. The fingers can be arranged in a compact interdigital fashion with common source and drain bonding pads. The total linear extent of the source or drain (if each of these were stretched out in one dimension) is a characteristic parameter, Z, the gate width. The program goal was to be able to switch 100 mA of current at up to 250°C. Based on past experience with other JFET devices of various current switching capability, a gate width of at least 0.4 cm was indicated for GaAs JFET's for this program. In order to have a margin of safety, JFET devices, having Z = 0.4 cm, 0.6 cm and 0.8 cm were constructed. (The actual layout of the designs is shown in Section 4.2, JFET and Diode Fabrication.) The three designs were placed on a single chip so that selection could be made of the optimum device which would be able to switch the required current at 250°C and at the same time have low off-state leakage currents. Final device selection was based on curve-tracer current-voltage characteristics. The reason for using the smallest value of Z which is consistent with switching requirements is to reduce JFET off-state junction and surface leakage currents which increase with Z. This has beneficial effects in photoswitch circuit design which leads to a reduction in optical power requirements at the phototransistor. At the time of device design, an off-state gate leakage current of under 100 μA was expected at 250°C for a GaAs JFET with Z = 0.4 cm at 20V stand-off and -12V on the gate.

For turbine-engine electronic control applications, the digitally controlled power device must switch current into an inductive load. In order to protect the semiconductor switch against inductive voltage buildup and subsequent device failure when current is turned off, an alternate low-impedance return path must be available to the coil decay current. One way to protect the switch is to place a diode across the inductive load. For high-temperature application a GaAs junction diode is preferred. A GaAs Zener diode would be more difficult to fabricate, and a Schottky barrier device may be susceptible to long-term reliability problems due to metal-semiconductor interactions. With current flowing in the actuator coil, the diode is under reverse bias. When the JFET current switch turns off, the diode provides protection against inductive voltage buildup by being forced into forward bias so that inductive current circulates through the diode and coil and allows only an extra diode forward voltage, about 1V to 2V, to appear at the JFET drain. The energy is therefore dissipated in the diode and the coil. The peak energy dissipation rate is reached very quickly after the switch is opened and diminishes exponentially thereafter with the characteristic time constant.

The layer structure for the transient-protection diodes used in this program was of the $p^+/n/n^+$ type as in the case of the JFET (see Fig. 3-2). Diode processing was simpler since only one top-surface contact to the n^+ layer was required. The n-layer carrier concentration was decreased to about $6 \times 10^{15} cm^{-3}$ to provide a safe 50V reverse bias capability (20V is the power supply voltage). From Eq. 3-3, at least 3.4 μm of n-GaAs is required for this carrier concentration. One factor that enters into diode mesa-size selection is the maximum allowable temperature rise above ambient that can be tolerated. Device diameter can be estimated using

$$\Delta T = \frac{P_d \ell_s}{K \pi r_d^2} \qquad (3\text{-}4)$$

where ΔT is the steady-state temperature rise, P_d is the power to be dissipated, ℓ_s is the distance through the GaAs substrate to an infinite heat sink, K is the thermal conductivity of GaAs (0.35 watt/cm/°C at 250°C) and r_d is the radius of the diode. If 0.1A of current is switched at 100 Hz through a torque-motor coil with an inductance of 0.1 Henry, then 0.05 watt must be dissipated through the coil and diode. If all of the power were dissipated through the diode, then a maximum of a 190-μm-diameter mesa diode (ℓ = 200 μm) would be required for a temperature rise of 10°C. For this program a range of mesa diameters, 76 μm to 320 μm, was fabricated on a single chip. Selection of the proper size was also based on keeping the transient-voltage buildup at the JFET drain to 2V or below over the -54°C to 250°C

application range. Compared to coil activation currents, diode reverse-bias leakage currents were expected to be small, i.e., less than 15 μA at a 20V reverse bias for a 250-μm-diameter mesa at 250°C.

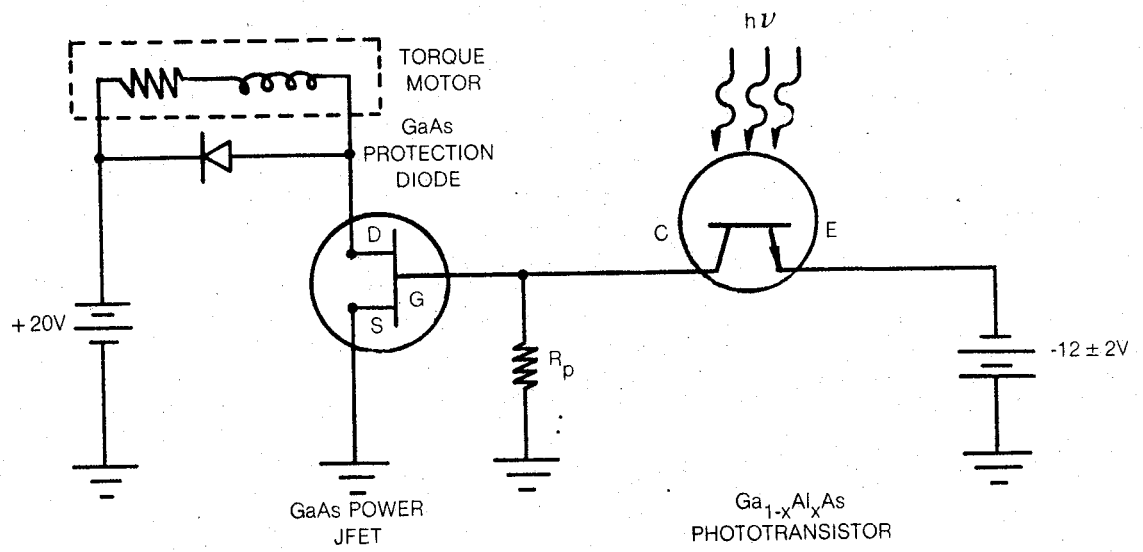
Two configurations for placement of the phototransistor and power device with respect to each other for pulse-width modulation of current into a torque motor are shown in Fig. 3-3. In both cases, the current through the coil is determined by the voltage on the GaAs JFET gate from a separate power supply. At near-zero voltage on the gate, the power device is on and the coil is activated. If a negative voltage in the range of -10V to -14V appears on the JFET gate, current through the coil is switched off. As negative voltage increases on the JFET gate, the transient-protection diode will ensure that the JFET drain does not rise more than 1V to 2V above the power supply voltage. Digital electronic pulsing of the JFET gate can be accomplished with optical pulses from a fiber striking the surface of the phototransistor. Phototransistor placement can be either in series (Case I) or parallel (Case II) with the JFET gate. When the phototransistor is illuminated in Case I, the power switch will be in the off-state; in Case II, the optically activated phototransistor causes the JFET switch to allow current flow through the coil. Both of these cases were considered in the design phase of this program; however, Case II represents a more logical cause-and-effect relationship and was used on the breadboard.

As part of the design phase, photoresponse measurements were made on formerly fabricated UTRC phototransistors between room temperature and 250°C. This information provided a basis for circuit design in this section of the report and design of the optical path in Section 3.2. Current-voltage characteristics at 250°C for a 300-μm-diameter phototransistor are shown in Fig. 3-4. When used with the JFET switch, the phototransistor should supply photocurrent with minimum internal voltage drop; therefore, the current at the knee of each of the curves is the maximum allowable current. The knee phototransistor voltage drop was near 1V when illuminated with 100 to 200 μW of radiation. In Fig. 3-5, the knee photocurrents (corrected for about 50 μA of dark current at the knee voltage) are plotted versus illumination after an initial stabilization period of a few hours at 200 to 250°C. Optical gain (calculated from the photocurrent data) is shown in Fig. 3-6. Device optical gain is defined as the ratio of the photocurrent, I_p, to the incident photon flux,

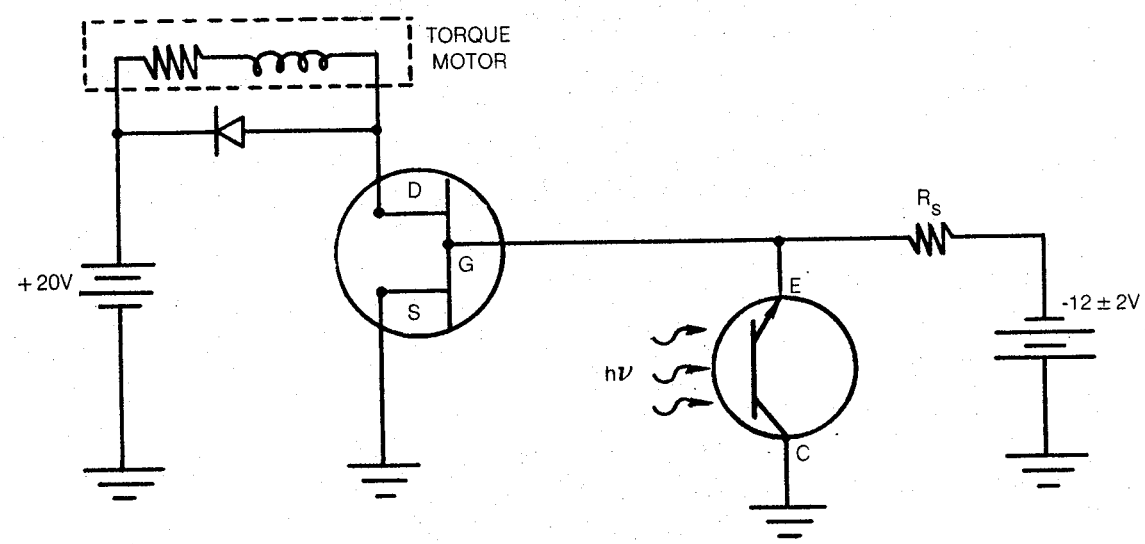
$$g = \frac{I_p h\nu}{q\ P_o} \qquad (3\text{-}5)$$

GaAs DEVICE CONFIGURATIONS FOR OPTICAL SWITCHING

CASE I. LIGHT ON → POWER SWITCH OFF



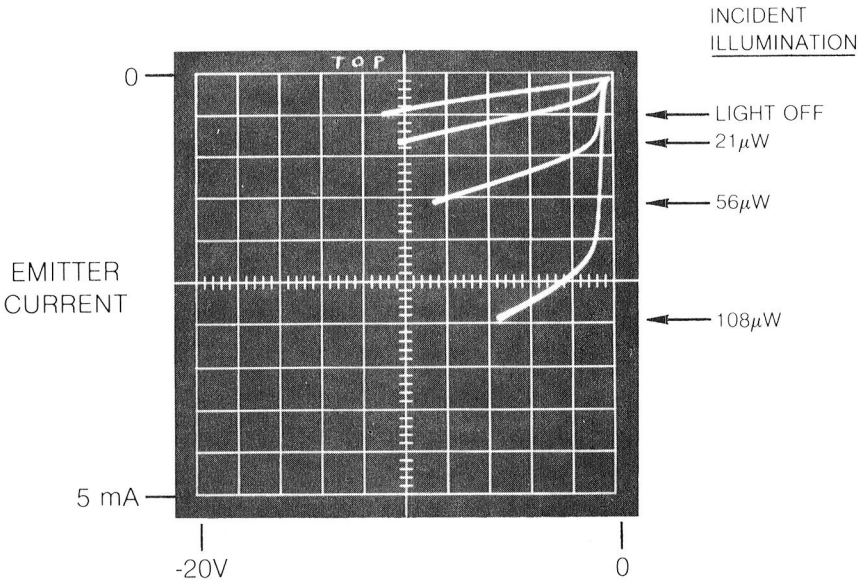
CASE II. LIGHT ON → POWER SWITCH ON

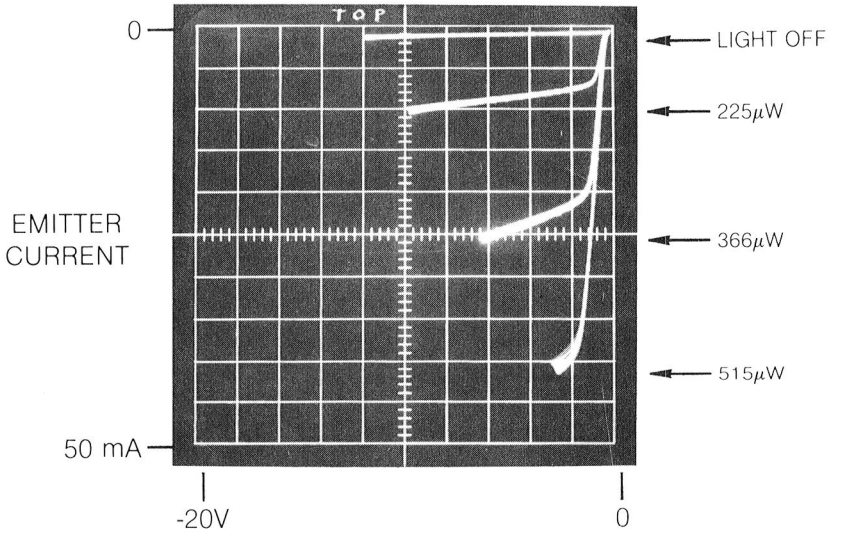


80-03-42-20

PHOTOTRANSISTOR CHARACTERISTICS AT 250°C

BASE FLOATING — COLLECTOR GROUNDED
DEVICE 6-10
$\lambda = 8104\text{Å}$



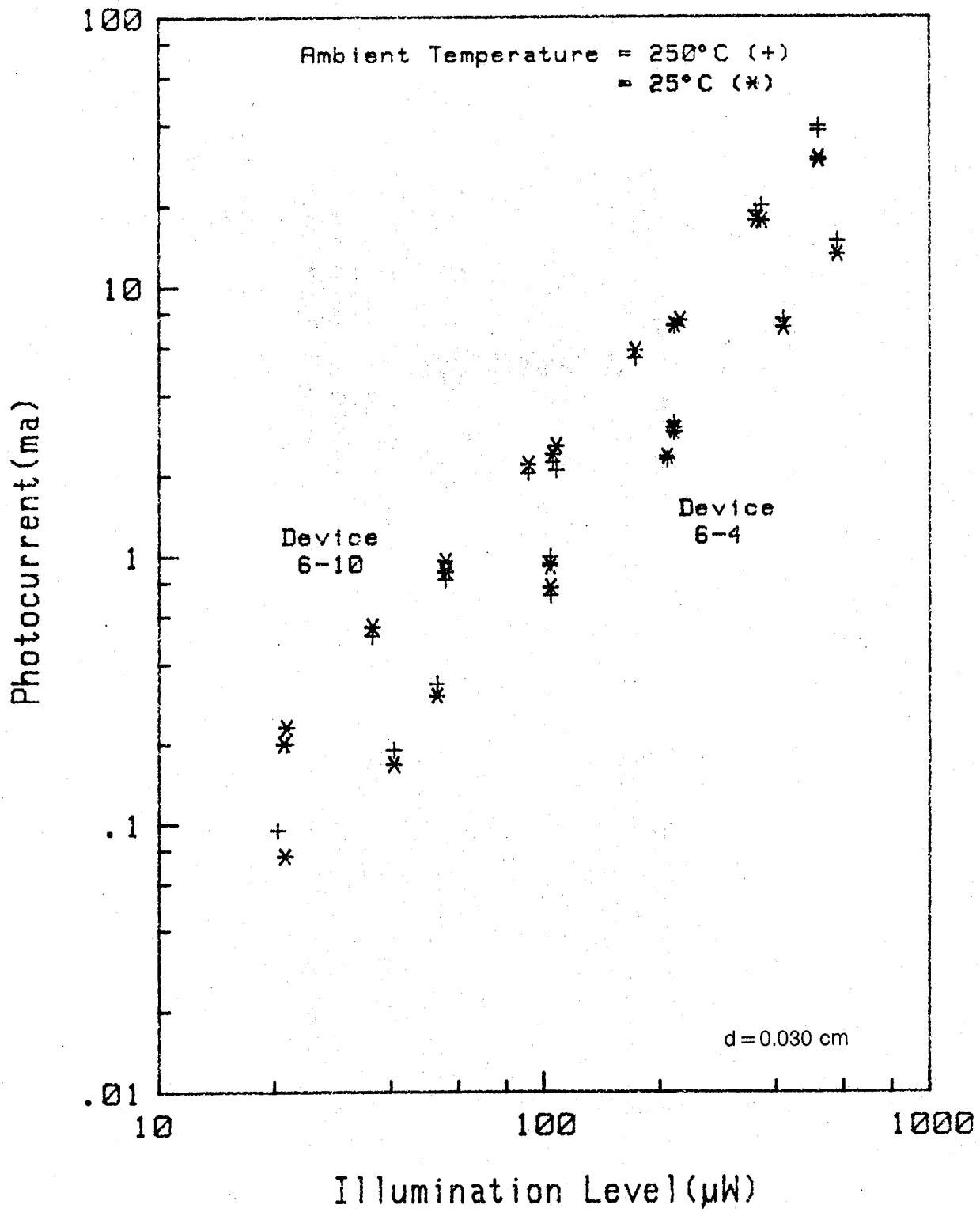


EMITTER VOLTAGE

80—10—9··2

FIG. 3-5

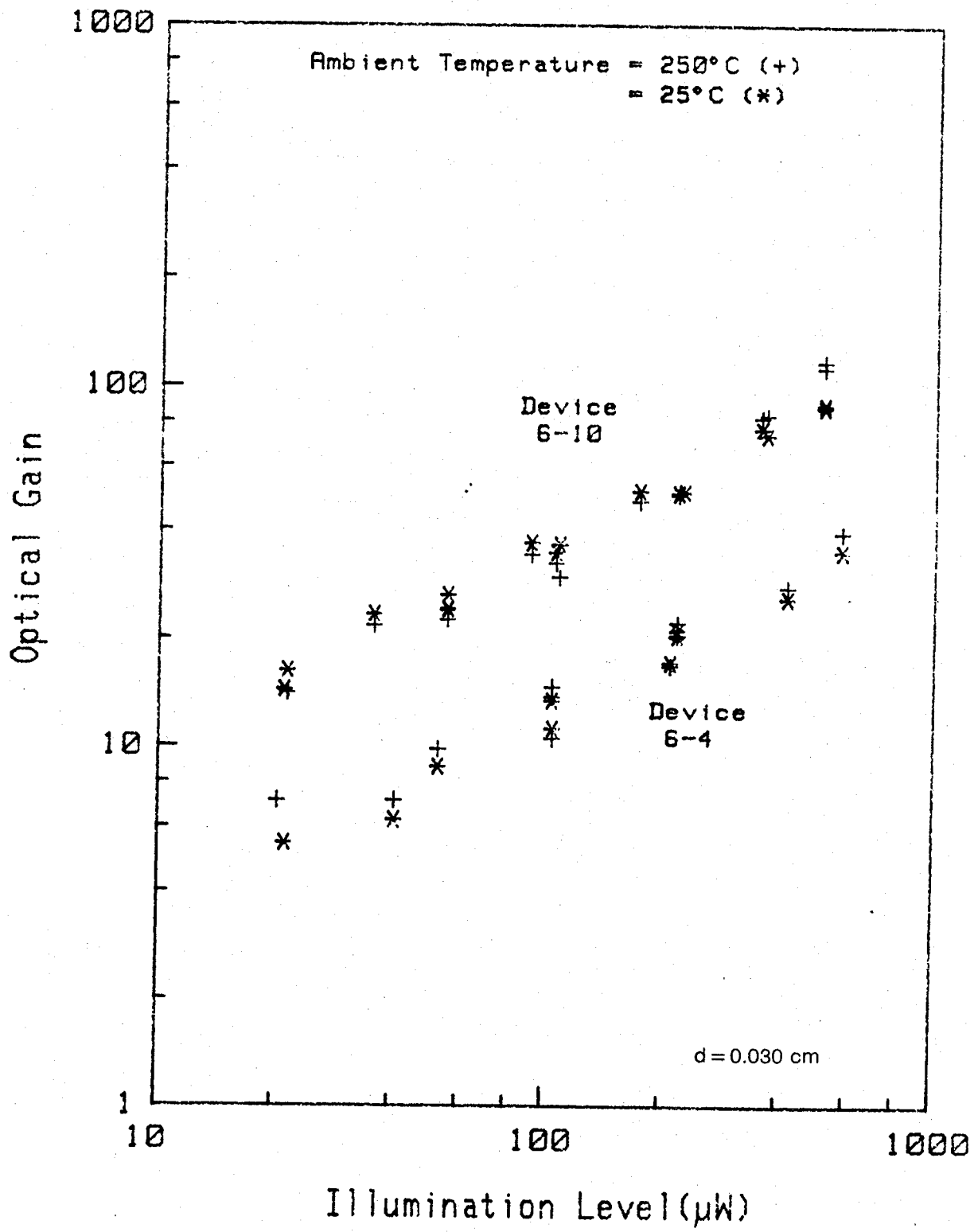
GaAs PHOTOTRANSISTOR CHARACTERISTICS
KNEE PHOTOCURRENT VS ILLUMINATION



80-10-9-6

FIG. 3-6

GaAs PHOTOTRANSISTOR CHARACTERISTICS
KNEE OPTICAL GAIN VS ILLUMINATION



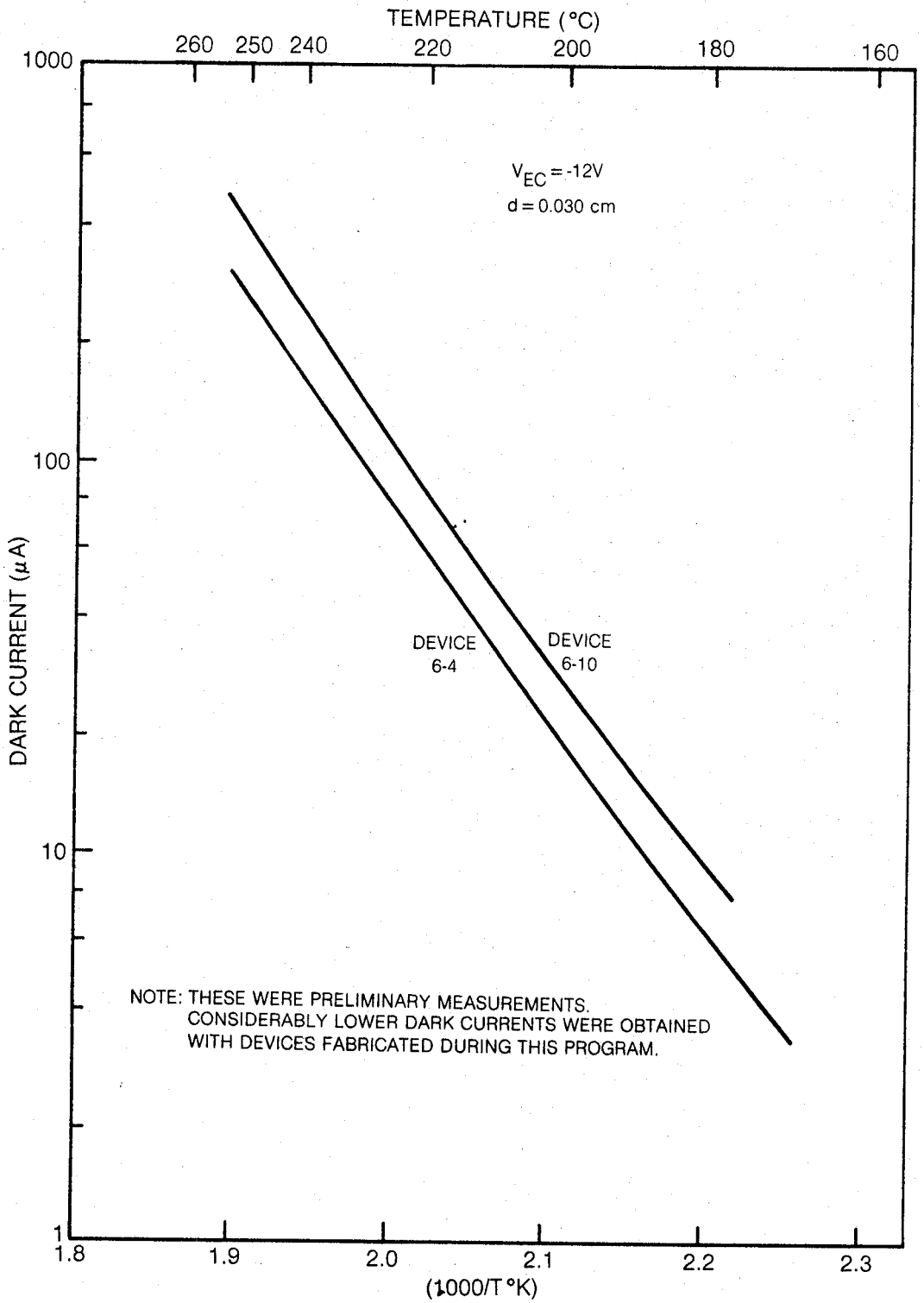
80-10-9-7

where P_o is the incident optical power of frequency, ν. As can be seen, there are only small differences in response over the temperature range for each device; similar results were expected down to -54°C. The increase in gain with illumination level is characteristically observed in GaAlAs heterojunction phototransistors. This dependence suggests that the smallest diameter phototransistor should be used in order to reduce the required optical power. One phototransistor parameter that undergoes large changes with temperature is the dark current, which is shown in Fig. 3-7 for two test devices at a bias level of -12V (V_p of JFET). During phototransistor operation, the optically generated current as well as the ordinary bulk reverse-bias junction currents are multiplied by the transistor gain. Measured dark currents for phototransistors fabricated during this program were significantly reduced from the values shown in Fig. 3-7. These larger values are attributed to additional surface or defect contributions.

The phototransistor dark current at the highest operational temperature (250°C) is an important parameter in circuit design since this represents the lowest off-state dc resistance for the device; therefore, the value of R_p or R_s in Fig. 3-3 must be adjusted using this value to assure proper switching over the entire temperature range. In Case I, with no illumination, about a 12V drop will exist across the phototransistor and near-zero voltage will be on the JFET gate if the off-state dc resistance of the phototransistor is much greater (> 10X) than the net resistance of R_p in parallel with the JFET gate resistance (R_G) to ground. When the phototransistor is illuminated, it must supply current through R_p to bring the JFET gate to near -12V. This will take place if the phototransistor can deliver a knee current of $12/R_p$ plus an expected JFET gate current of 100 μA. The knee photocurrent response curves (Fig. 3-5) can then be used to establish the minimum optical power required at the phototransistor. In Case II with no illumination, a -12V pinch-off voltage will be on the JFET gate if the net resistance to ground of the two devices is much greater (> 10X) than R_s. When sufficient optical power is incident on the phototransistor, current ($\sim 12/R_s$) is shunted to ground and most of the -12V power supply is dropped across R_s, low voltage appears on the JFET gate, and current flows into the coil.

Phototransistor dark current scales with junction area. Since junction area includes active and inactive (bonding pad) regions, dark current will decrease more slowly than the inverse-diameter-squared dependence. From a circuit viewpoint, it is advantageous to use the smallest phototransistor diameter to reduce dark current, increase R_p or R_s and therefore reduce optical power requirements. Assuming that device gain depends on illumination density as obtained from Fig. 3-6, the minimum required illumination levels for phototransistors #6-10 and #6-4 can be calculated as a function of mesa diameter for each circuit configuration of Fig. 3-3. For purposes of these calculations, the JFET on-state and off-state voltages were taken to be -1V and -11V respectively, R_G = 120 K ohms, and the bonding pad area was 6 x

PHOTOTRANSISTOR DARK CURRENT



80–10–9–1

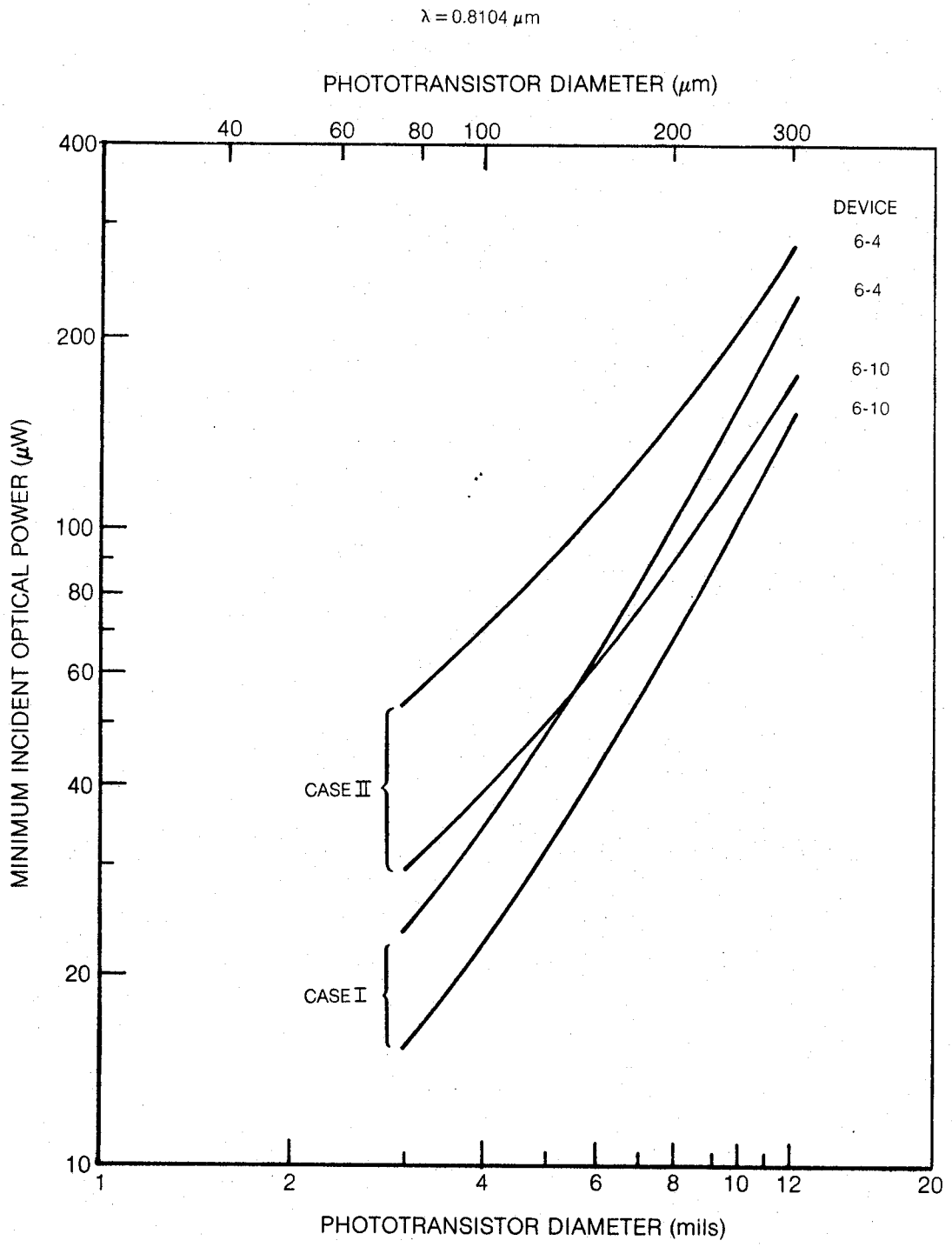
$10^{-5}cm^2$. The resistor values, R_p and R_s, depended on phototransistor geometry and dark currents. The results are shown in Fig. 3-8. The differences between the two phototransistors are related to differences in gain and dark currents. The Case-II configuration requires more phototransistor illumination than for Case I. Smaller phototransistor diameters are favored to reduce optical source power; however, other factors such as available photon flux, packaging, and on-state phototransistor voltage drop will moderate the trend to smaller phototransistor diameters. In part of the next section, the principal limiting factor, optical power density at the phototransistor, will be discussed in relation to Fig. 3-8 to finally determine phototransistor size.

3.2 Design of the Optical Path

The requirements of the program included a breadboard demonstration system which utilized fiber optic cable, connectors, a light source, power supplies for the light source, and high-temperature GaAs devices mounted on the breadboard. A schematic of the optical path for delivering optical power to the phototransistor is shown in Fig. 3-9. Two connectors were utilized to connect source and detector pigtails to the transmission cable for ease of component replacement. The optical cable had to be at least 6 meters in length. This section addresses elements of the photoswitch design that involve the optical path; i.e., light source to phototransistor. Factors considered were choice of source, coupling of source to fiber, optical fiber choice, coupling of fiber to phototransistor, and system optical loss. These factors were also used in determining phototransistor size.

The fly-by-light optical source must be capable of delivering optical power to the phototransistor at the levels shown in Fig. 3-8. GaAs-type solid-state devices are good choices for this application because (1) optical power levels can be met with a single fiber with reasonable efficiency, (2) pulse-width modulation of the source is easily done, and (3) source lifetimes are long, i.e., 10^4 hours for an ILD (Injection Laser Diode) and 10^5 hours for an IRED (InfraRed Emitting Diode). The wavelengths of interest are between 0.80 and 0.84 μm. In this region the phototransistor surface $Ga_{1-x}Al_xAs$ layer ($x = 0.2$ to 0.4) acts as a window for absorption of radiation in the underlying GaAs base and collector regions. ILD's can easily meet the phototransistor optical power requirements. The IRED is preferred because it is more economical, easier to use, has longer life, and can operate in a higher temperature environment compared to the ILD. The photoswitch circuit requirements are such that a high-radiance IRED source is required to meet the optical power levels shown in Fig. 3-8. Based on literature survey of possible IRED's, the Hitachi series of high-radiance domed HLP devices was selected for breadboard use. These devices were supplied uncapped so that at UTRC an optical fiber had to be coupled to the domed GaAlAs material surrounding the emitting region.

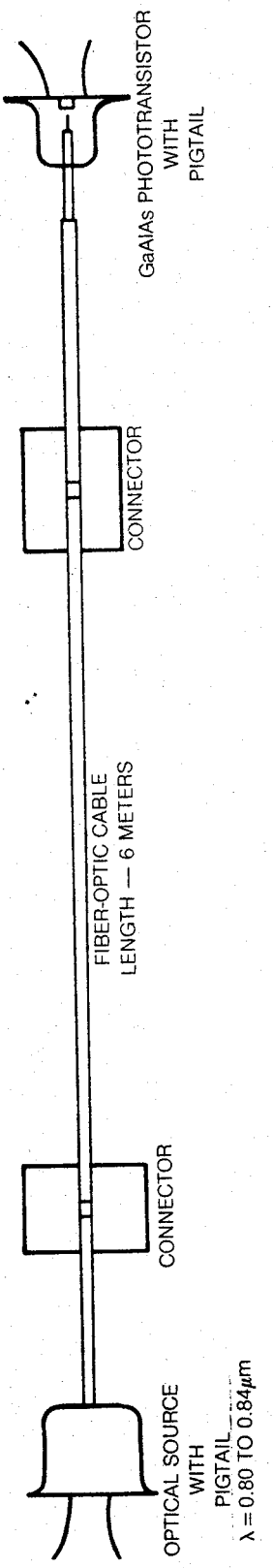
MINIMUM INCIDENT OPTICAL POWER AT PHOTOTRANSISTOR



80–10–59–5

FIG. 3-9

SCHEMATIC OF OPTICAL PATH



80-10-59-6

The efficiency of optical coupling to an IRED increases with core cross-sectional area (for core area less than the IRED emitting area) and the square of the fiber numerical aperture (NA). Maximum power transfer to the phototransistor using a single fiber will occur if a high-NA, large-diameter fiber is butted against the IRED source at one end and the same-diameter phototransistor at the other end. For optical coupling to the IRED, a fiber can be positioned to within 25 μm of the top of the IRED dome. At the phototransistor, additional clearance had to be allowed in the hermetic sealing process (this will be described later in this section). If such a clearance is required, some optical power will be lost at the phototransistor unless the phototransistor diameter exceeds the fiber diameter. Increasing phototransistor diameter arbitrarily is not desired since circuit phototransistor optical requirements from Fig. 3-8 must increase.

Multimode optical fibers with high numerical aperture and constructed using glass core and cladding are available with core diameters of 100 μm and 200 μm. It was required in this program that the fiber had to survive in both the maximum ambient application temperature and maximum process temperature for phototransistor hermetic sealing. For commercially available optical cables, the cable materials must be stripped from the length of fiber that will be in hot zone. Table II summarizes room-temperature characteristics of applicable optical fibers as well as expected connector losses.

TABLE II

PROPERTIES OF OPTICAL FIBERS

Fiber #	Fiber Core Diameter (μm)	Fiber NA	Fiber Attenuation (λ=8200 Å) (dB/km)	Estimated Connector Loss (dB/Connector)
A	200	0.55/0.5	12	1
B	200	0.4/0.35	35	1
C	100	0.55/0.5	12	1.5
D	100	0.3/0.28	7	1.5

Using data supplied by the IRED manufacturer, a summary of maximum values for optical power that can be coupled into each fiber core as well as power available at the fiber end for the phototransistor after cable and connector losses are accounted for is shown in Table III. The highest predicted power coupling efficiency is 5% for the high-NA, 200-μm-diameter fiber (A in Item 1). The Item-2 optical powers can be fully utilized if phototransistor area is at least as large as the illuminated area.

TABLE III

MAXIMUM COUPLED AND AVAILABLE OPTICAL POWER
USING IRED SOURCES

Item	Optical Fiber	IRED		
		HLP-60	HLP-50	HLP-40
1. Estimated coupled power into fiber core.	A	3.1 mW	2.6 mW	2.1 mW
	A*	--	2.2	--
	B	1.7	1.4	1.1
	C	0.81	0.68	0.54
	D	0.25	0.21	0.17
2. Calculated power available for phototransistor	A	1.9	1.6	1.3
	A*	--	1.2	--
	B	1.0	0.84	0.67
	C	0.41	0.33	0.27
	D	0.13	0.10	0.08

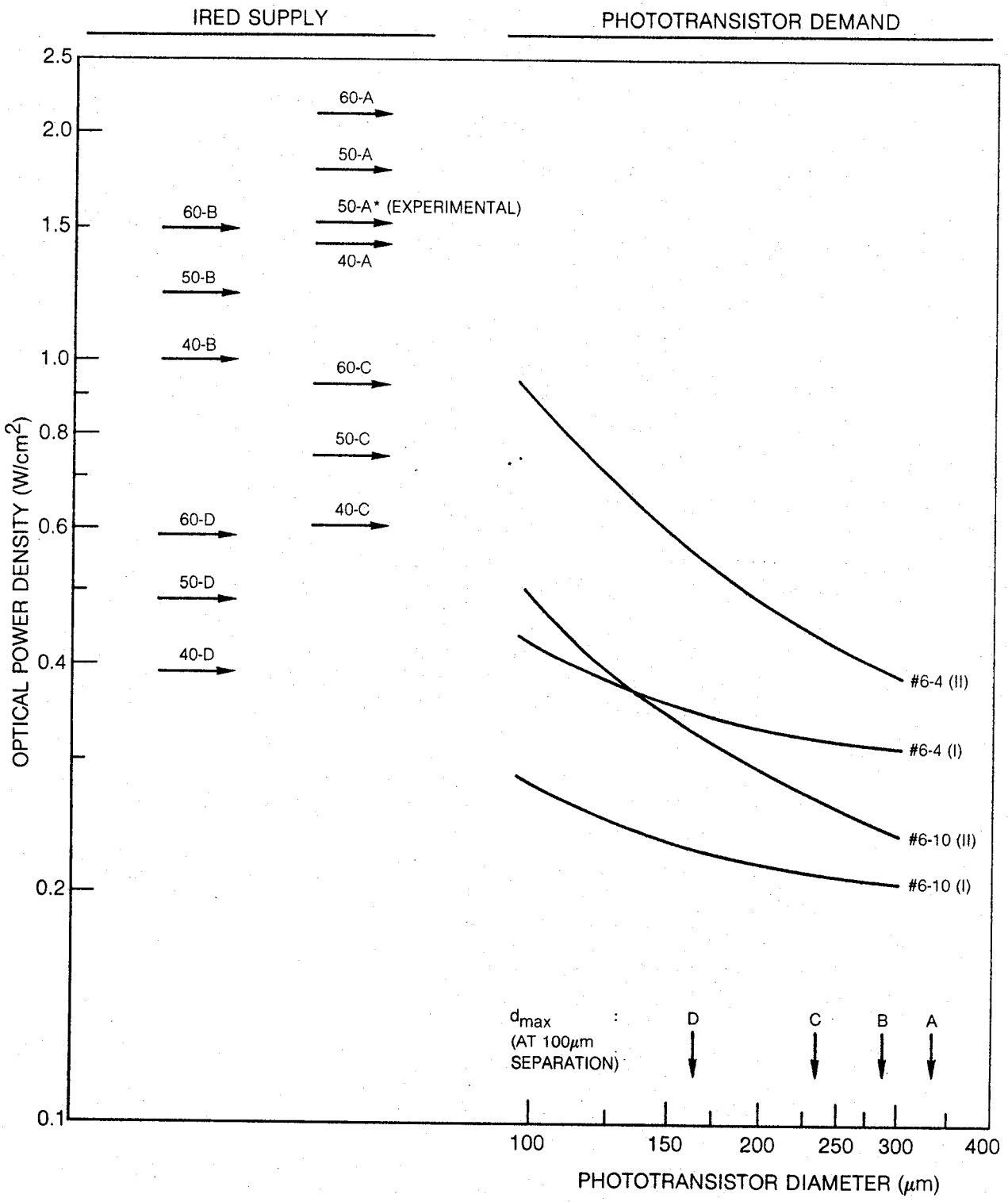
* measured at UTRC

If the phototransistor can be reproducibly positioned 100 μm from the optical fiber in device packaging and sealing, the available optical power density (assumed to be uniform) at the plane of the phototransistor can be compared with required phototransistor optical density as calculated from Fig. 3-8 for the two circuit configurations of Fig. 3-3. Figure 3-10 compares the supply optical power density levels, established by the various IRED-fiber combinations, at the phototransistor with the phototransistor demand values.

FIG. 3-10

SUPPLY AND DEMAND OPTICAL POWER DENSITIES

SUPPLY CALCULATED FOR PHOTOTRANSISTOR-FIBER SEPARATION OF 100μm



83-3-119-2

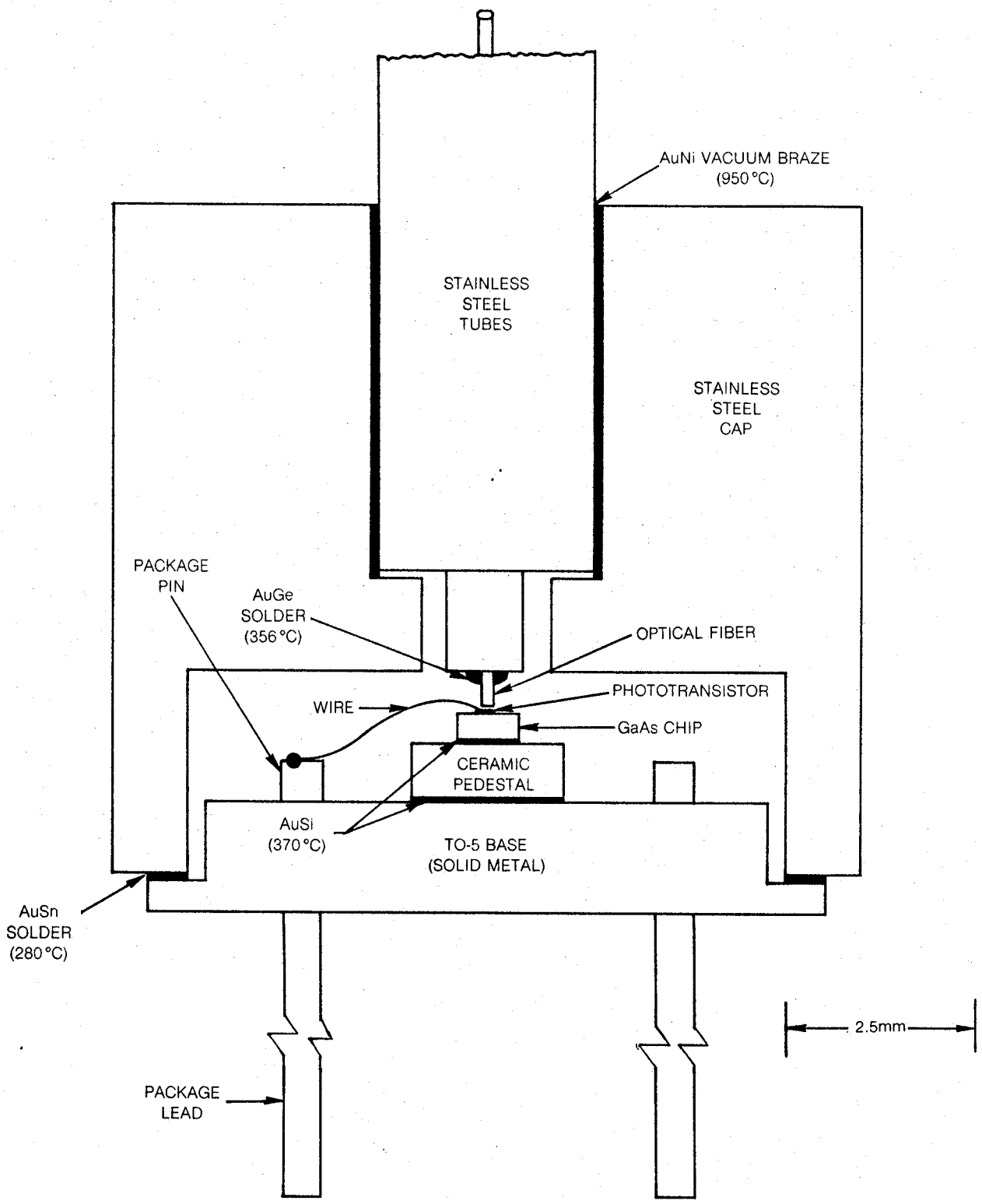
With the 200-μm-diameter fibers (A and B) there appears to be sufficient optical power available using the IRED's. The minimum phototransistor diameter should be 200 μm since smaller diameters could not utilize all the light emerging from the fiber in the limit of butt-coupling. As determined from the fiber NA, the maximum phototransistor diameter (d_{max}) or the diameter of the light-cone base 100 μm away from the fiber end, is greater than 290 μm as shown in Fig. 3-10.

With the 100-μm-core fibers, sufficient optical density may be available for use with smaller-diameter phototransistors. In evaluating this option the following factors were taken into account: (1) allowance had to be made for the fact that the IRED supplied optical power densities in Fig. 3-10 are maximum values, (2) the preferred Case-II circuit approach required higher optical power, (3) as phototransistor diameter decreases below about 150 μm and photocurrent density and gain increase, knee voltage drops greater than one volt can exist across the phototransistor. This is not desired for the Case-II parallel-gate configuration in order to keep the onstate gate condition for the JFET between 0 and -1V.

In view of the above considerations and the facts that optical density gradients will be present at the edges of the light cone and fiber positioning may be closer than 100 μm, the phototransistor diameter chosen for breadboard use was 200 μm. The chosen fiber was Fiber A since this had a higher-temperature strain point than Fiber B and, therefore, was preferred for high-temperature sealing and use. Also, Fiber-A attenuation did not change more than 0.002 dB between -60°C and 80°C; higher-temperature data were not available from the manufacturer. In the final packaging of the phototransistor with fiber-optic pigtail (described below), only about 8 cm of fiber had to be exposed to the -54°C to 260°C ambient; therefore, additional fiber attenuation was expected to be negligible.

The design for packaging the phototransistor with the fiber optic pigtail is shown in Fig. 3-11. The package had to be able to withstand long-term ambient temperatures of up to 250°C and had to be hermetically sealed to avoid environmental contamination of exposed phototransistor junctions along the mesa edge. High-temperature epoxy was not used inside the device package because of possible long-term high-temperature outgassing which could degrade device performance. A cleaner sealing technique using high-temperature brazing to a metallized fiber was adopted. The final pieces to be joined were (1) a standard TO-5 package with a mounted and wired phototransistor and (2) a cap assembly that guided and protected a bare optical fiber which was metal coated at the end and sealed into place. Eutectic brazes used were AuNi, AuSi, and AuGe, and a final seal (with device-fiber alignment) was made with the lowest temperature eutectic, AuSn (280°C). The goal was a helium-leak-tight package with the fiber positioned precisely over the phototransistor and to within 100 μm of the phototransistor surface.

PHOTOTRANSISTOR PACKAGING SYSTEM



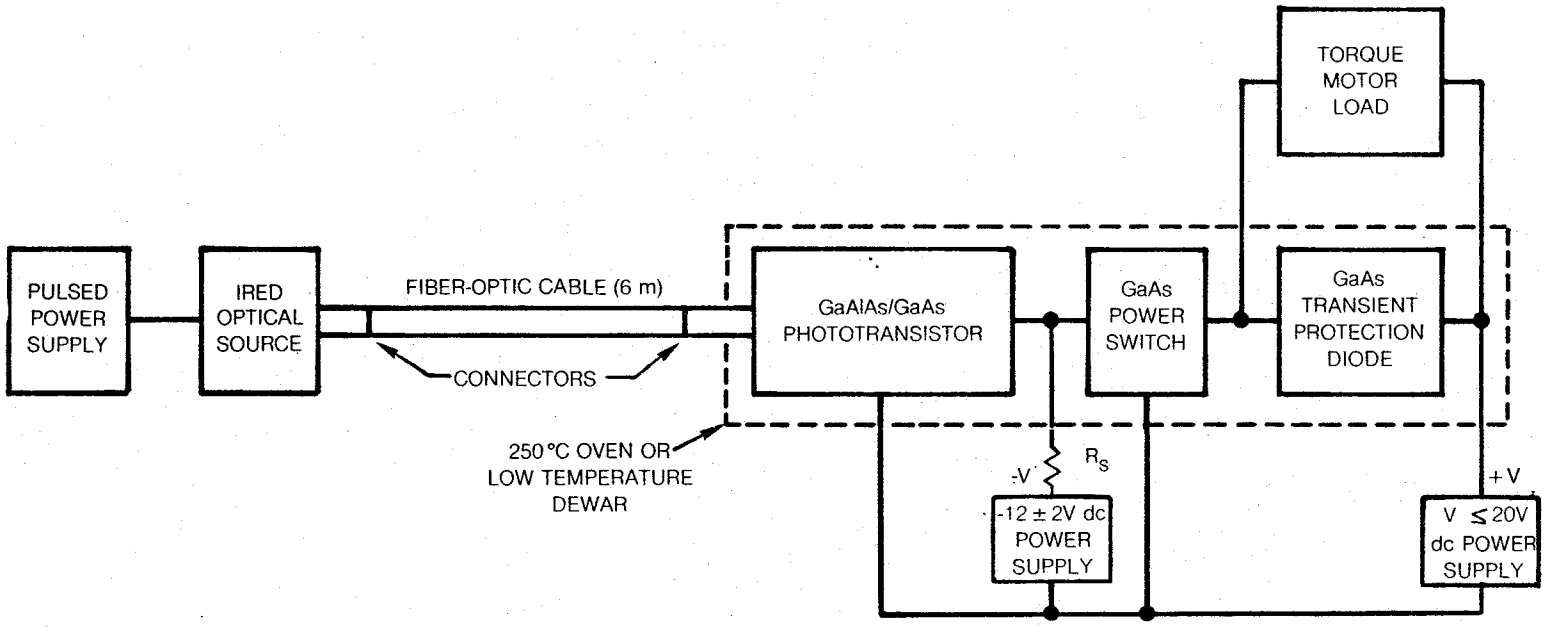
81–5–17–2

3.3 Design Aftermath

The photoswitch devices that were fabricated and tested to demonstrate fiber optic high-temperatures switching into actuator loads were a GaAlAs/GaAs phototransistor (photosensitive device), a GaAs JFET (100 mA power switch), and a GaAs diode (transient-protection device). The phototransistor was an N/p/n bipolar transistor which was operated as a two-terminal device (base floating). Upon illumination with near-infrared radiation from an optical source (λ = 0.8 to 0.84 μm) the phototransistor exhibited gain and was used to trigger the GaAs JFET into switching current into a torque-motor load. Both the JFET power switch and transient-protection diode had a p^+-n structure. The JFET was a three-terminal device with surface interdigital fingers comprising the source and drain and with p^+ substrate as gate. This device was normally-on unless pinched-off with a gate voltage of -10 to -14V. Each of the photoswitch devices was fabricated by sequentially growing the epitaxial layers on a GaAs substrate and processing the wafers. Device sizes were as follows: phototransistor (mesa diameter of 200 μm); diode (mesa diameter under 250 μm); and JFET (Z = 0.4 cm to 0.8 cm). All devices were much faster than maximum expected pulse-width-modulation frequencies.

As a result of phototransistor gain measurements and expected losses in the optical path, an IRED was used as the optical source on the breadboard. A schematic diagram incorporating the essential items of the breadboard demonstrator is shown in Fig. 3-12. The phototransistor was placed in the parallel-gate configuration so that optical excitation resulted in activation of the torque motor. Both the light source and phototransistor required a fiber optic pigtail which connected to the transmission cable. Each GaAs device was hermetically sealed to avoid environmental contamination of GaAs exposed junctions and possible device degradation. Special procedures were required for simultaneous sealing and alignment of the phototransistor with the optical fiber. The breadboard configuration allowed full testing of the photoswitch system at ambient temperatures between -54°C and 250°C.

BREADBOARD BLOCK DIAGRAM



4.0 PHOTOSWITCH FABRICATION

The GaAs epitaxial layers required for fabrication of phototransistor, JFET and diode structures were grown using liquid-phase epitaxy (LPE) at United Technologies Research Center (UTRC). Use was made of a transient-mode technique based on one first reported by Deitch (Ref. 13) together with a GaAs LPE tilt system. For specific details on LPE system description, GaAs epitaxial-growth procedures and material characterization, see Ref. 14. All fabrication steps including preparation of photolithographic masks, wafer processing and device packaging were carried out at UTRC.

4.1 Phototransistor Fabrication and Packaging

A schematic diagram of the high-temperature-capability phototransistor in cross section was shown in Fig. 3-1. This device required growth of two GaAs layers and one GaAlAs layer on an n^+-GaAs substrate. These layers formed the device collector, base and emitter respectively. The collector layer had to be 3 μm thick to fully absorb the IRED radiation. The base layer had to be as thin as possible (~ 0.5 μm), and the required aluminum atom fraction, x, in the emitter layer was to be between 0.2 and 0.4. Layer carrier concentrations and Hall mobilities inferred from data taken on layers in adjacent growth runs are shown in Table IV for two wafers which were the source of phototransistors for this program. Layer thicknesses, obtained from either near-infrared reflection spectroscopy or microscopic fringe measurements, are also listed.

TABLE IV

PHOTOTRANSISTOR EPITAXIAL-LAYER DATA

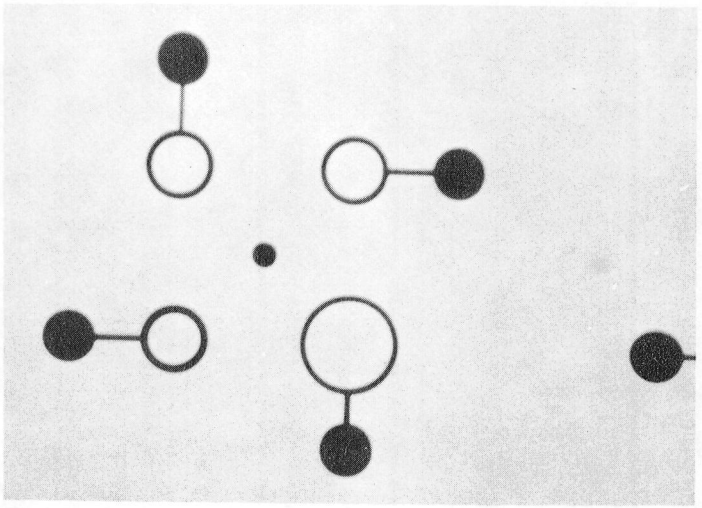
Wafer	Layer	Thickness (μm)	Carrier Density (cm^{-3})	Hall Mobility at 298°K ($cm^2V^{-1}sec^{-1}$)
W1	Collector	3.9	$n = 1.9 \times 10^{16}$	5650
	Base	≤ 0.5	$p = 1.2 \times 10^{18}$	140
	Emitter (x=0.3)	1.8	$N = 5 \times 10^{17}$	1600
W2	Collector	4.5	$n = 1.9 \times 10^{16}$	5650
	Base	≤ 0.7	$p = 1.2 \times 10^{18}$	140
	Emitter (x=0.3)	2.0	$N = 4 \times 10^{17}$	1400

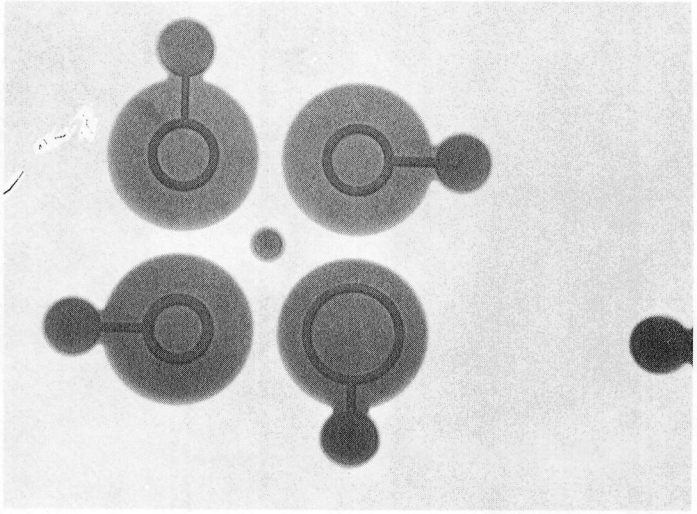
Three photolithographic masks were required for phototransistor processing. These provided (1) emitter Au-Ge alloyed rings, (2) Au metallization build-up and bonding pad formation, and (3) mesa (island) etching to isolate devices. Figure 4-1 shows top surface views of four slightly different phototransistor structures that were fabricated. The upper photo gives the result of a double exposure alignment test generated on an emulsion plate using the step-and-repeat camera and first-reduction plates for the first two process masks. The Au-Ge mask consisted of circular contact rings with each device utilizing one ring. Alternating phototransistor cells also had an associated Au-Ge 60-μm-diameter pad for each device for extra alloying underneath the wire contact. The gold-build-up mask had 5-μm wider rings as well as 70-μm-diameter pad areas and interconnecting metallization. Some variations in ring width and ring diameter were utilized in order to ascertain any effects on final device performance. As discussed in Section 3.2, phototransistors having a diameter of 200 μm were required for this program. The lower photograph shows an alignment test using a triple exposure of the three process masks. The large-diameter circular areas define the active surface area of each phototransistor. The gold metallization is contained within each of the mesa areas. The bonding pad is the device emitter contact; the collector is the substrate. Only one of the four devices was coupled to a fiber optic pigtail in the final sealing to the cap assembly.

The important phototransistor processing steps are illustrated with schematic cross-sectional views in Figs. 4-2 and 4-3. The process headings include (1) definition of contact areas, (2) front ohmic-contact metallization, (3) gold build-up, (4) ring and pad formation and thinning of the quartz anti-reflection layer, and (5) phototransistor isolation. Individual steps made use of sputtering to apply the various metallizations and quartz, three photoresist steps for device definition, chemical and plasma etching of quartz and removal of photoresist, ion milling of thick (2 μm) gold, alloying for 10 minutes at 420°C and chemical etching of GaAs. The quartz was required to provide a stop for ion milling of the thick gold and serve as a convenient anti-reflection layer in the finished device. Figure 4-4 shows top-surface views of finished devices on the wafer.

Prior to packaging, phototransistors were probed for electrical and optical performance. Devices exhibiting the highest optical gain and proper dark current-voltage characteristics were cleaved from the parent wafers. Each GaAs chip was mounted onto a ceramic pedestal onto a TO-5 solid metal base. The phototransistor packaging procedure required that each GaAs die be located to within 0.25 mm of the center of the TO-5 package base. The die was positioned in XY using a cross hair in a binocular eyepiece attached to the die bonder. Based on room temperature optical response, dark electrical characteristics and appearance, the best phototransistor on each die was contacted using thermocompression bonding of gold wires (25-μm diameter) at the device bonding pad, package pins, and surface gold film on the ceramic

PHOTOTRANSISTOR STRUCTURES





80–12–18–1

PHOTOTRANSISTOR PROCESSING

DEFINITION OF CONTACT AREAS

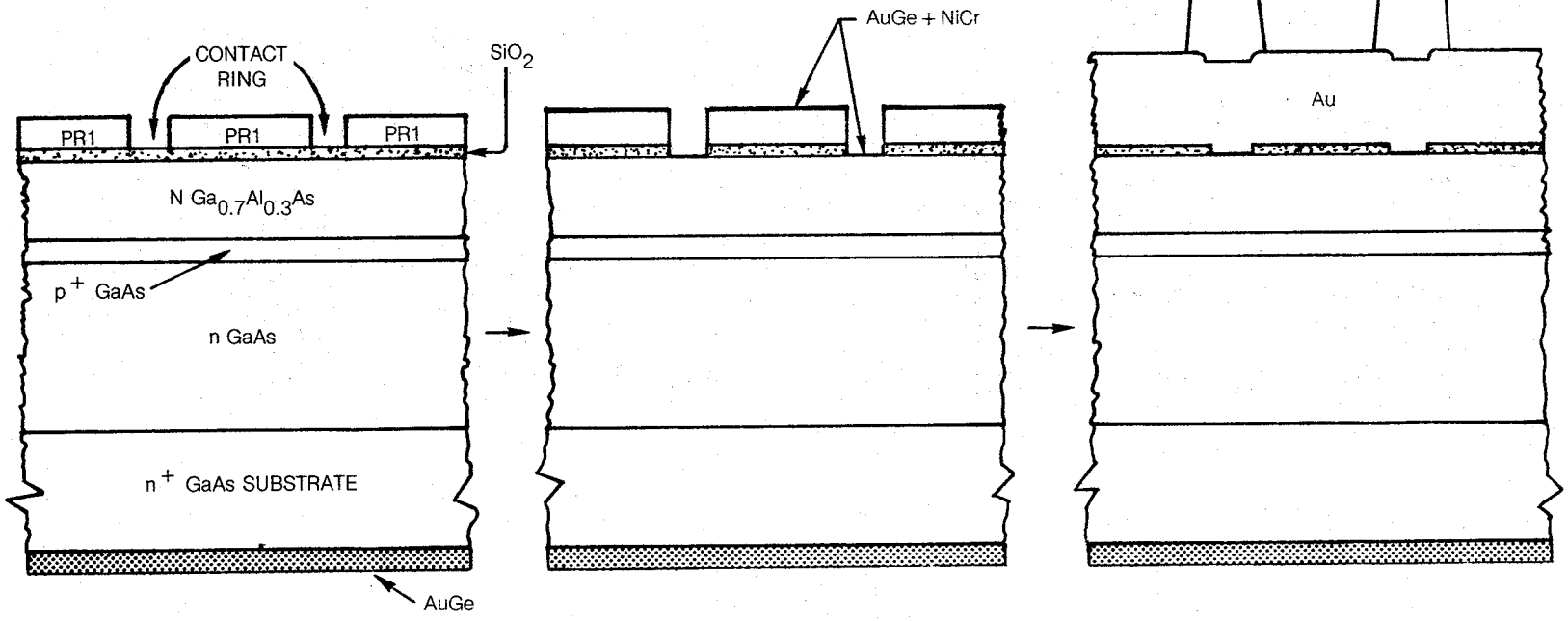
1. GROW THREE EPITAXIAL LAYERS
2. SPUTTER 0.2μm SiO_2
3. SPUTTER AuGe ON BACK SIDE OF SUBSTRATE
4. PR SiO_2 (PR1)

FRONT OHMIC-CONTACT METALLIZATION

6. SPUTTER AuGe + NiCr

GOLD BUILD-UP

9. SPUTTER NiCr AND THICK Au
10. PR Au (PR2)



5. ETCH SiO_2

7. LIFT OFF PR1, EXTRA AuGe, AND NiCr
8. ALLOY AuGe

1μm

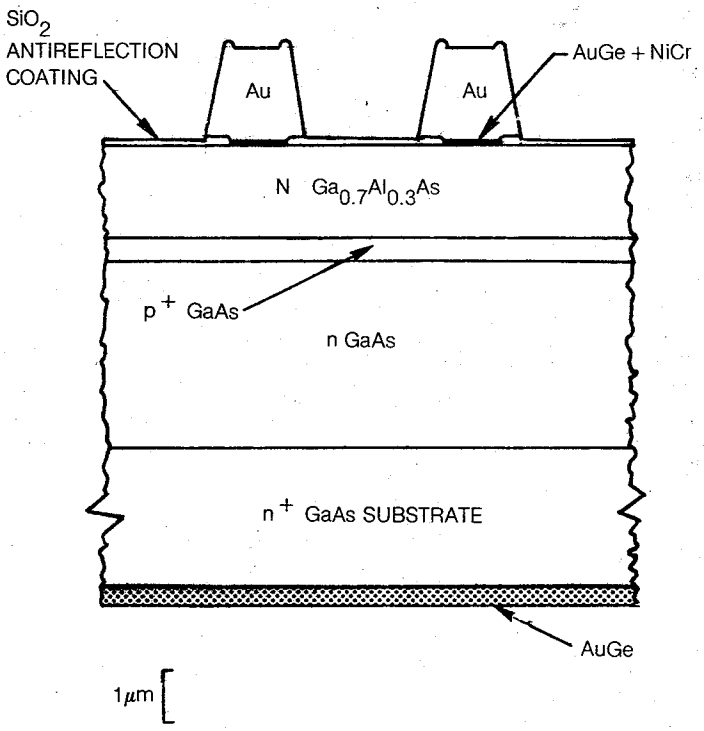
PHOTOTRANSISTOR PROCESSING (CONTINUED)

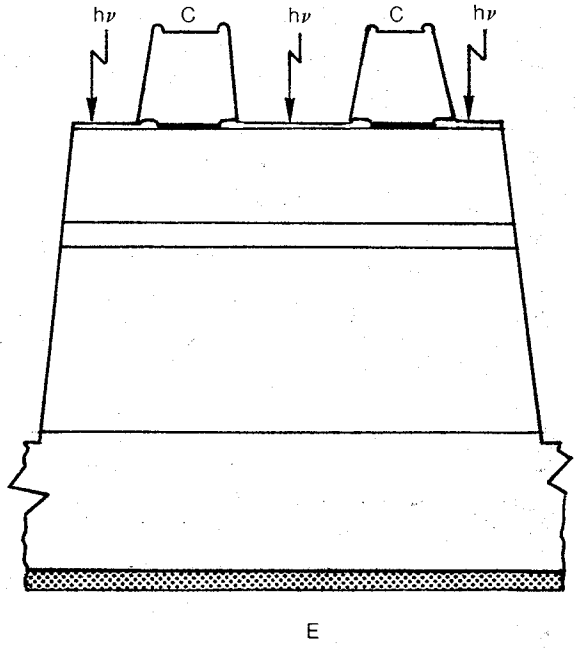
RING AND PAD FORMATION AND SiO_2 THINNING

11. ION MILL Au AND PR2
12. TRIM SiO_2 TO ~1400Å THICK
13. REMOVE LEFTOVER PR2

DEVICE ISOLATION

14. PR DEVICE MESA (PR3)
15. ETCH SiO_2 BETWEEN DEVICES
16. ETCH GaAs BETWEEN DEVICES
17. REMOVE PR3

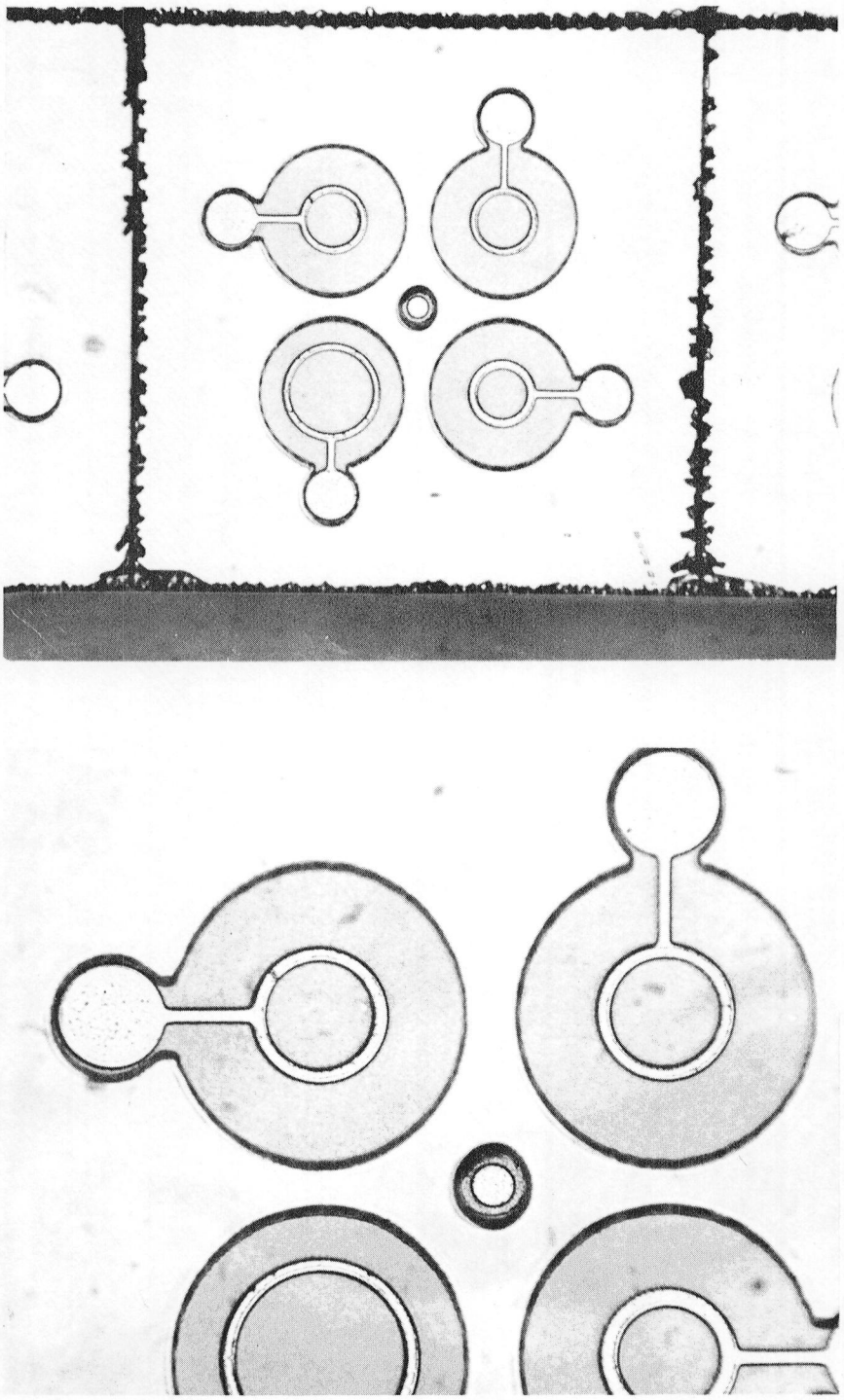




E

18. TEST DEVICES ON WAFER
19. SCRIBE AND CLEAVE WAFER
20. PACKAGE AND SEAL WITH CAP AND FIBER OPTIC PIGTAIL

ON-WAFER PHOTOTRANSISTORS



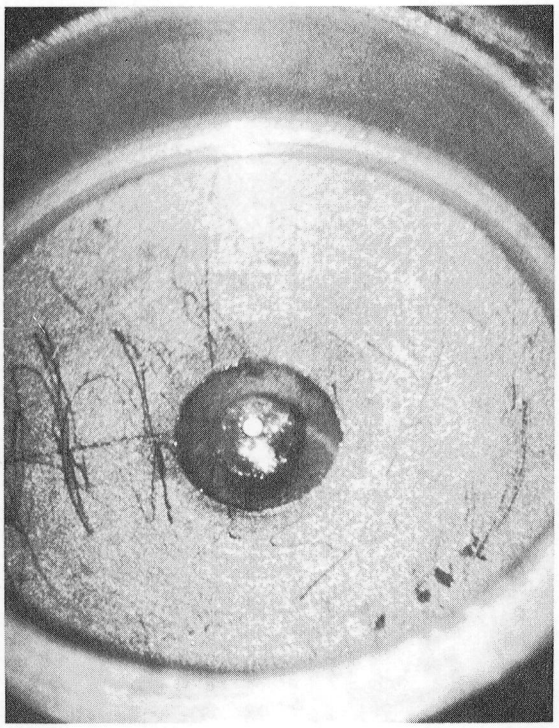
DEVICE DIAMETER = 200μm

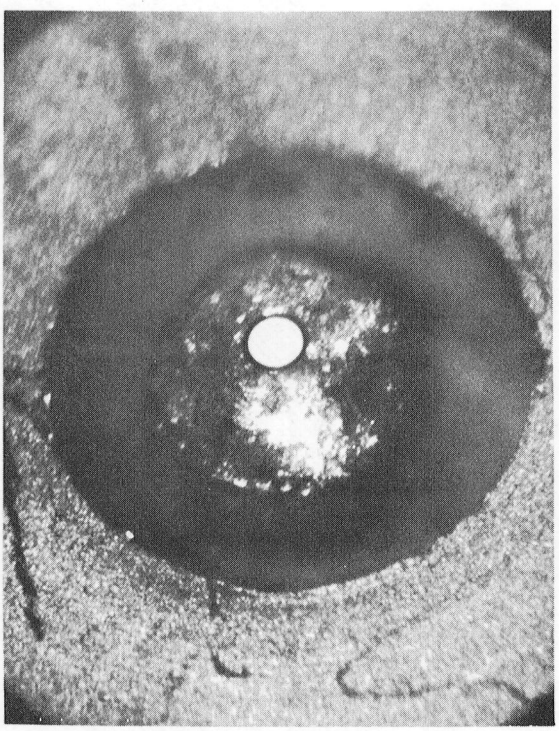
83–3–119–5

pedestal. Before final sealing, measurements had to be made of the distance (Z direction) from the surface of the phototransistor to the plane of the rim of the TO-5 package as well as the maximum height of the wire above the phototransistor surface. For the delivered devices the maximum wire heights ranged between 45 μm and 65 μm above the phototransistor surface. The optical fiber had to be positioned further away in order to avoid interference with the bonding wire. Mounted phototransistors were further screened before capping by making high-temperature photoresponse measurements which are described in Section 5.1.

The overall design for packaging the phototransistor with the fiber optic pigtail for high-temperature application was shown in Fig. 3-11. The final step in the packaging procedure was to hermetically seal the specially prepared cap assembly, which guided and held the sealed optical fiber, to the TO-5 base with centered phototransistor. An important packaging goal was to seal the glass fiber to the innermost stainless steel tube using a high-temperature brazing technique. The fiber optic cable had an optical connector at one end. The other end was prepared by (1) striping off the outer jacketing materials to a length of about 21 cm, (2) metallizing the first few centimeters of the exposed fiber end (proprietary process) and (3) polishing the fiber tip. Successful handling of the long length of exposed fiber without breakage during stripping, mounting, metallizing the tip, demounting, polishing, insertion through the innermost stainless steel tube, and final brazing to the cap assembly was a difficult task. The concentric stainless steel tubes were previously vacuum brazed together and to the stainless steel cap using AuNi eutectic. A "pretinning" step using AuGe eutectic was required to prepare the inner wall of the tip of the smallest stainless steel tube. Also, gold had to be sputtered onto the sealing rim of the cap to enable later AuSn eutectic bonding to the TO-5 base. After passage through the tubes, the optical fiber was soldered into place using AuGe eutectic. The fiber extended from the tube a specified distance, as measured under a microscope, so that after sealing of the cap to the base, the calculated fiber-phototransistor separation would be 100 μm or less. The fiber seal was then helium-leak checked while still in place in the brazing fixture. The lowest detectable leak rate for the helium leak detector was 1×10^{-11} std cc/sec. If the seal were not leak tight, the AuGe eutectic was remelted and the sealing process repeated. The other end of the stainless steel tube containing the optical fiber would be near room temperature during breadboard testing. At this end the fiber and sheathing were held in place with an epoxy resin so that the fiber would be clamped at both ends of the stainless steel tubes. In the last step of preparation of the fiber and cap assembly, the fiber was placed under some compression while the epoxy cured in order not to have tensile fiber stress present when the phototransistor end was heated. Photographs showing an optical fiber sealed with AuGe eutectic inside a TO-5 cap assembly are shown in Fig. 4-5. In these photographs some light was coupled into the connector end so that the fiber core could be highlighted. The fiber tip was

METALLIZED FIBER SEAL IN TO-5 CAP ASSEMBLY





FIBER CORE DIAMETER: 200μm

at a proper height, 340 μm above the inside flat of the cap, for near-butt coupling with a matched phototransistor in the next step. In one experiment the integrity of a fiber seal was verified by absence of leakage at -57°C using the helium leak tester.

The final seal between cap assembly and phototransistor was carried out in a separate nitrogen filled chamber after a 1-hour vacuum baking of the phototransistor at about 150°C. The fiber was centered over the phototransistor by adjusting the cap position with respect to the stationary TO-5 phototransistor base using a heated micrometer stage. Alignment was accomplished by activating the phototransistor with light from the fiber and maximizing phototransistor response. The final seal was made with AuSn eutectic which had the lowest melting temperature of the solders used in this package. A photograph of a completed phototransistor package with fiber optic pigtail is shown in Fig. 4-6. A thermocouple was tac welded to the outside base of the TO-5 package to monitor testing temperatures below the 280°C AuSn eutectic temperature.

4.2 JFET and Diode Fabrication

The GaAs JFET's and transient-protection diodes were both of the $p^+/n/n^+$ type. The carrier concentration in the n-layer of the diode was lower in order to provide a safe 50V reverse-bias capability. Except for channel etching, processing for the two devices was quite similar. The n^+ capping layer served as a low-resistance contact layer with AuGu alloying. Tabular data on thickness and electrical properties of the GaAs layers for the source wafers are shown in Table V. At a carrier concentration of $9 \times 10^{15} cm^{-3}$, a 2.2-μm thick layer is required to support 33V across JFET gate and drain. For the diode only 3.4 μm of $6 \times 10^{15} cm^{-3}$ epitaxial material is required to support -50V.

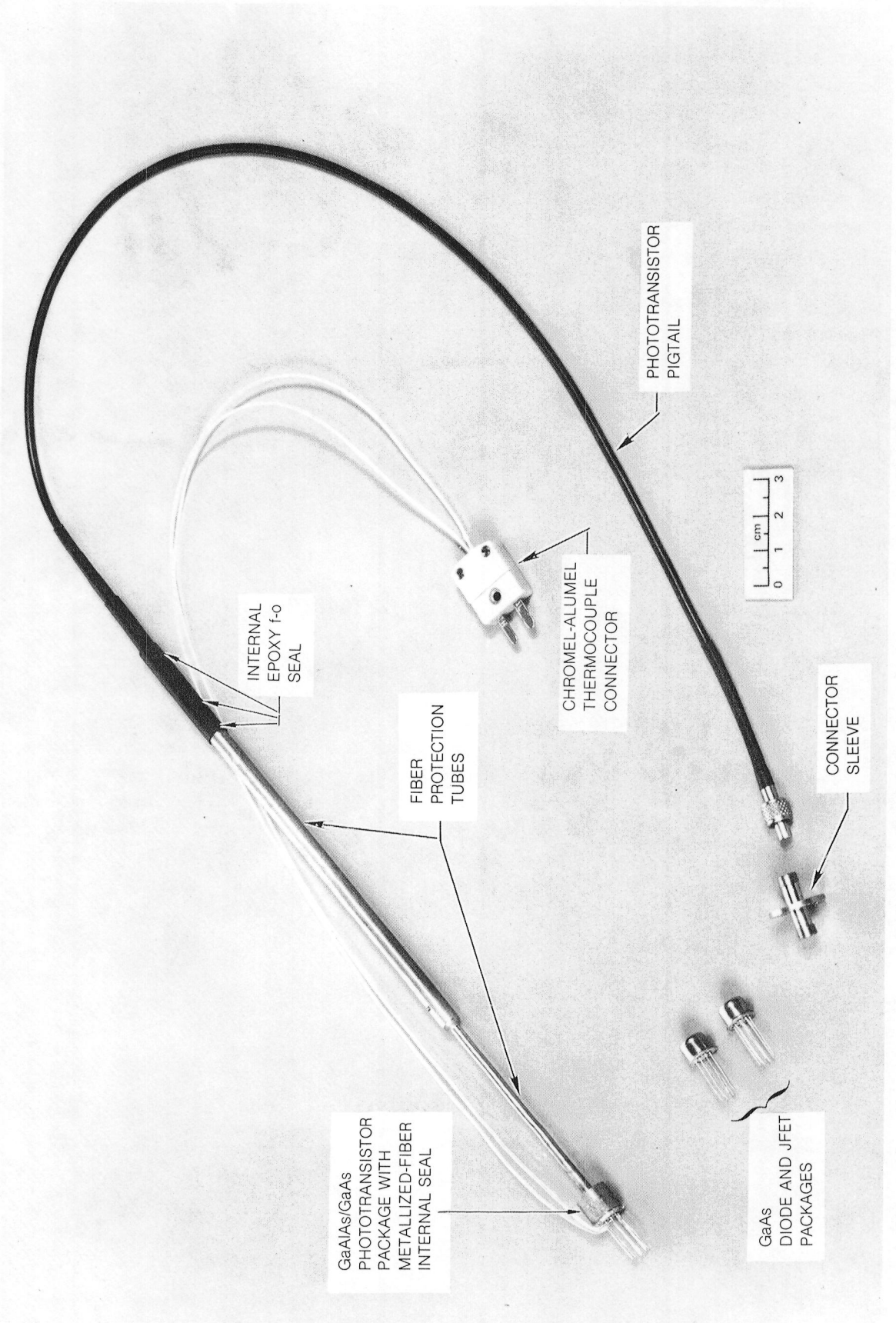
TABLE V

GaAs EPITAXIAL-LAYER DATA FOR JFET's AND DIODES

Wafer	Layer	Thickness (μm)	Electron Carrier Density (cm^{-3})	Hall Mobility at 298°K ($cm^2V^{-1}sec^{-1}$)
W3	n	2.7	9×10^{15}	6500
	n^+	1.2	8×10^{18}	--
W4	n	5.0	6×10^{15}	6400
	n^+	1.1	9×10^{18}	--

FIG. 4-6

PACKAGED PHOTOSWITCH DEVICES



82–203

82–6–103–2

Three photoresist masks were required for JFET and diode processing: (1) a mask for defining the AuGe contacts on the epitaxial layer surface, (2) another for establishing thick (~ 3 μm) gold to reduce metallization resistance, and (3) a final mask for mesa etching and isolation of devices. Figures 4-7 and 4-8 illustrate the design of three similar JFET structures fabricated on one chip for this program. The difference between the devices is the extent of interdigitation of source-drain finger pairs and therefore the current capacity of each. Since the source-drain spacing was constant, the junction area of each device varies. In Fig. 4-7, the pad and associated fingers towards the top of the photograph comprised the source for each device; the pad and fingers towards the bottom were the drain. The separation between source-drain fingers on the Au mask was designed to be 5 μm but the channel length (Fig. 3-2) was observed to be less than 3 μm after channel etching. The finger separation was increased at the tips in order to reduce electric fields and current flow in these areas. The width of a AuGe finger was 7.5 μm; the Au finger width was 12.5 μm. Final selection of the JFET to be used on a given die was based on the current-voltage curves of each device type. The designed gate width (Z) and junction area (a_j) for each of the devices of Fig. 4-7 (which from left to right are I, II, & III) are shown below:

TABLE VI

JFET MASK PARAMETERS

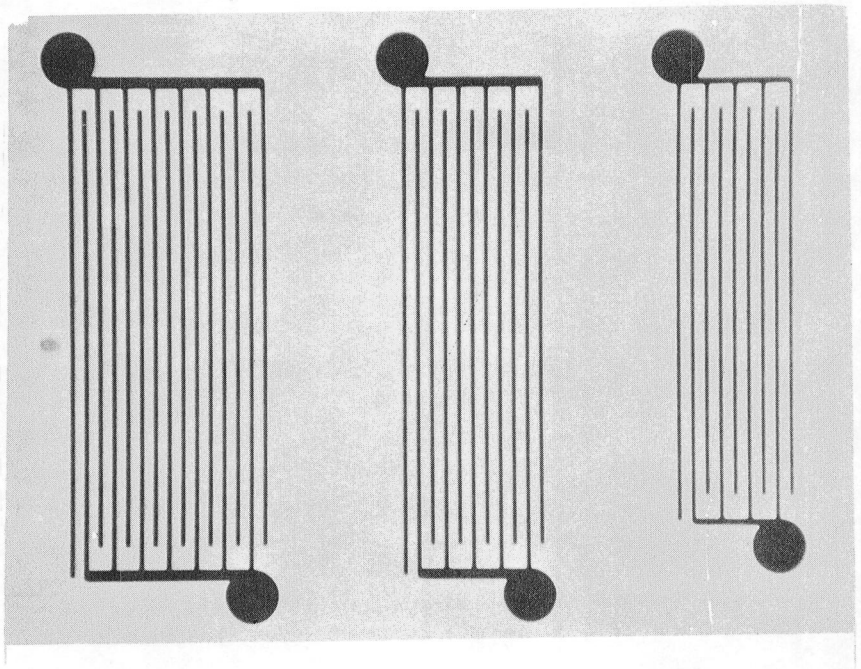
JFET Devices	Z (cm)	a_j (cm^2)
I	0.81	1.92×10^{-3}
II	0.58	1.44×10^{-3}
III	0.41	1.08×10^{-3}

The reason for using the smallest junction area consistent with switching requirements is to reduce JFET off-state junction leakage. This will increase the value of circuit resistance, R_s, in Fig. 3-3 and thereby reduce optical power requirements at the phototransistor.

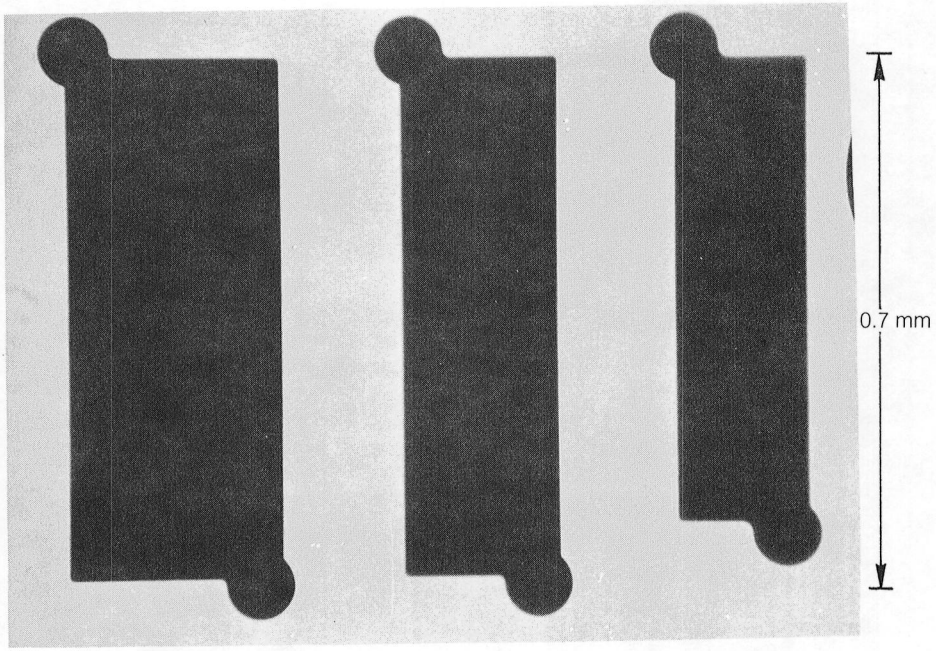
The important steps in JFET fabrication are illustrated with schematic cross-sectional views of a single finger pair in Figs. 4-9 and 4-10. The process headings include finger definition, ohmic-contact metallization, gold

PHOTOLITHOGRAPHIC MASKS FOR JFET SWITCH

Au-Ge MASK



MESA ETCH MASK

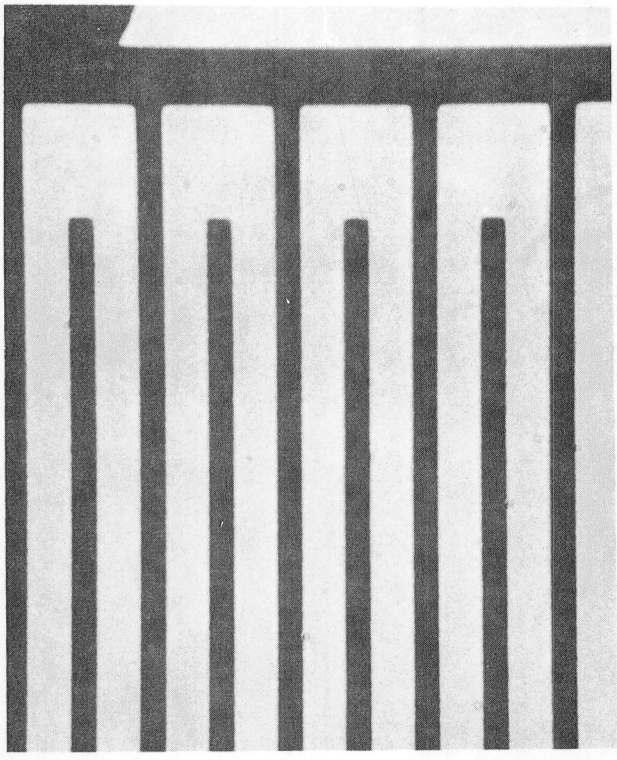


81–1–18–2

FIG. 4-8

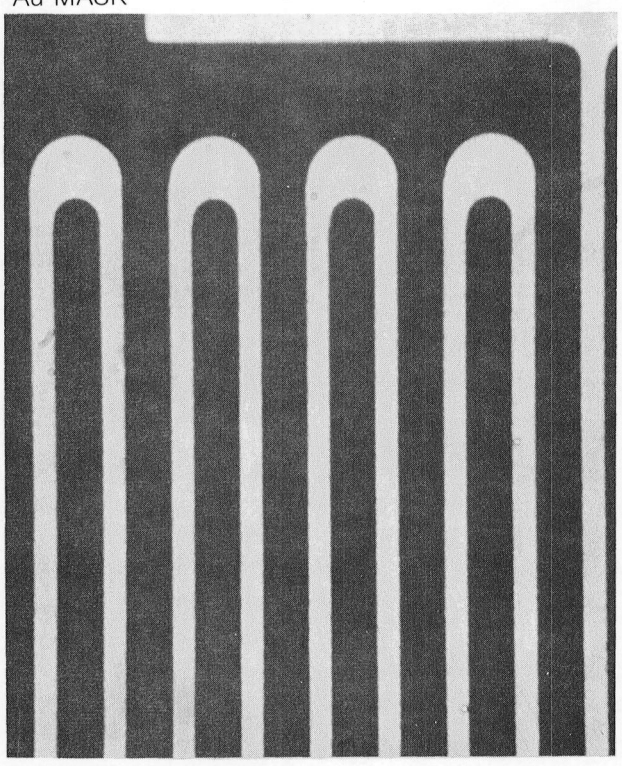
PHOTOMASK DETAILS FOR JFET SWITCH

Au-Ge MASK



50 μm

Au MASK



81–1–18–1

GaAs JFET PROCESSING

FINGER DEFINITION

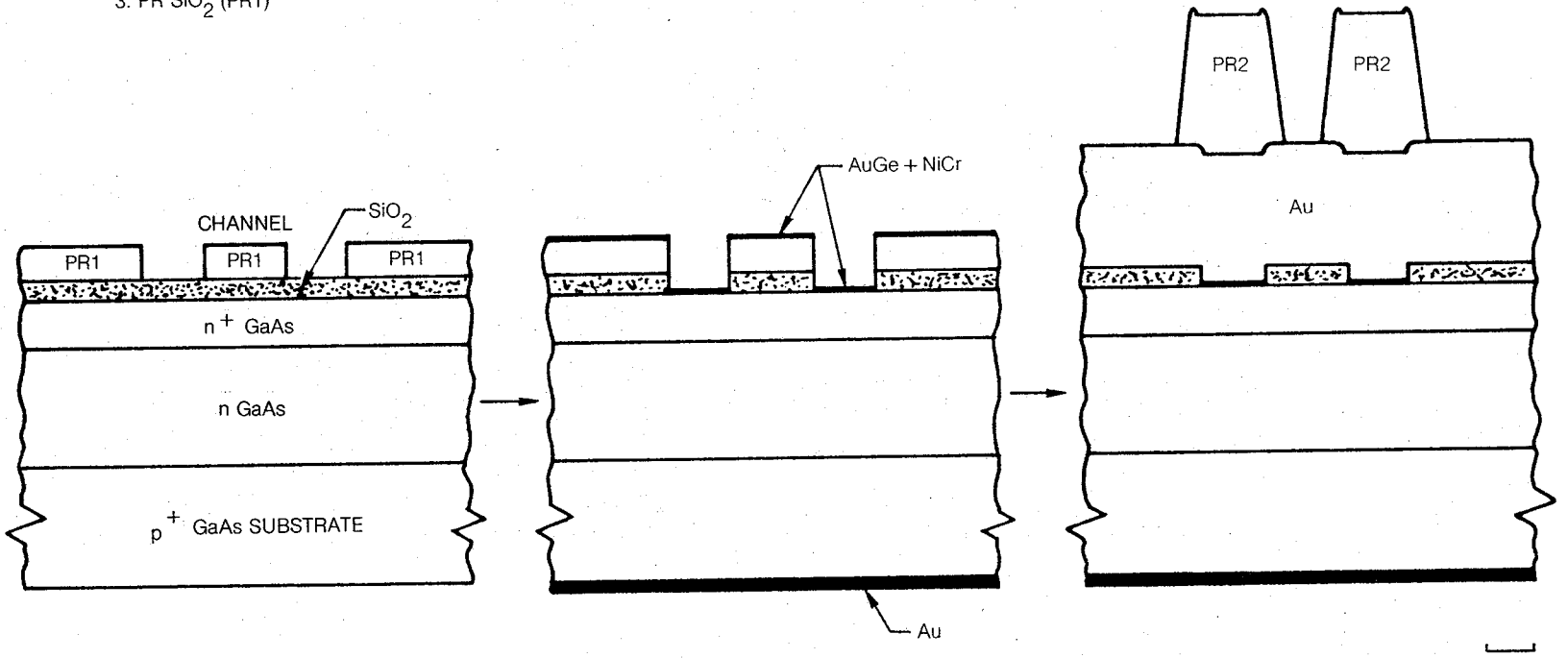
1. GROW TWO GaAs LAYERS
2. SPUTTER 0.5 μm SiO_2
3. PR SiO_2 (PR1)

OHMIC-CONTACT METALLIZATION

5. SPUTTER AuGe + NiCr
6. SPUTTER Au ON BACK SIDE OF SUBSTRATE

GOLD BUILD-UP

9. SPUTTER NiCr AND THICK Au
10. PR Au (PR2)



4. ETCH SiO_2

7. LIFT OFF PR1, EXTRA AuGe, and NiCr
8. ALLOY AuGe AND Au

FIG. 4-9

GaAs JFET PROCESSING (CONTINUED)

FINGER FORMATION

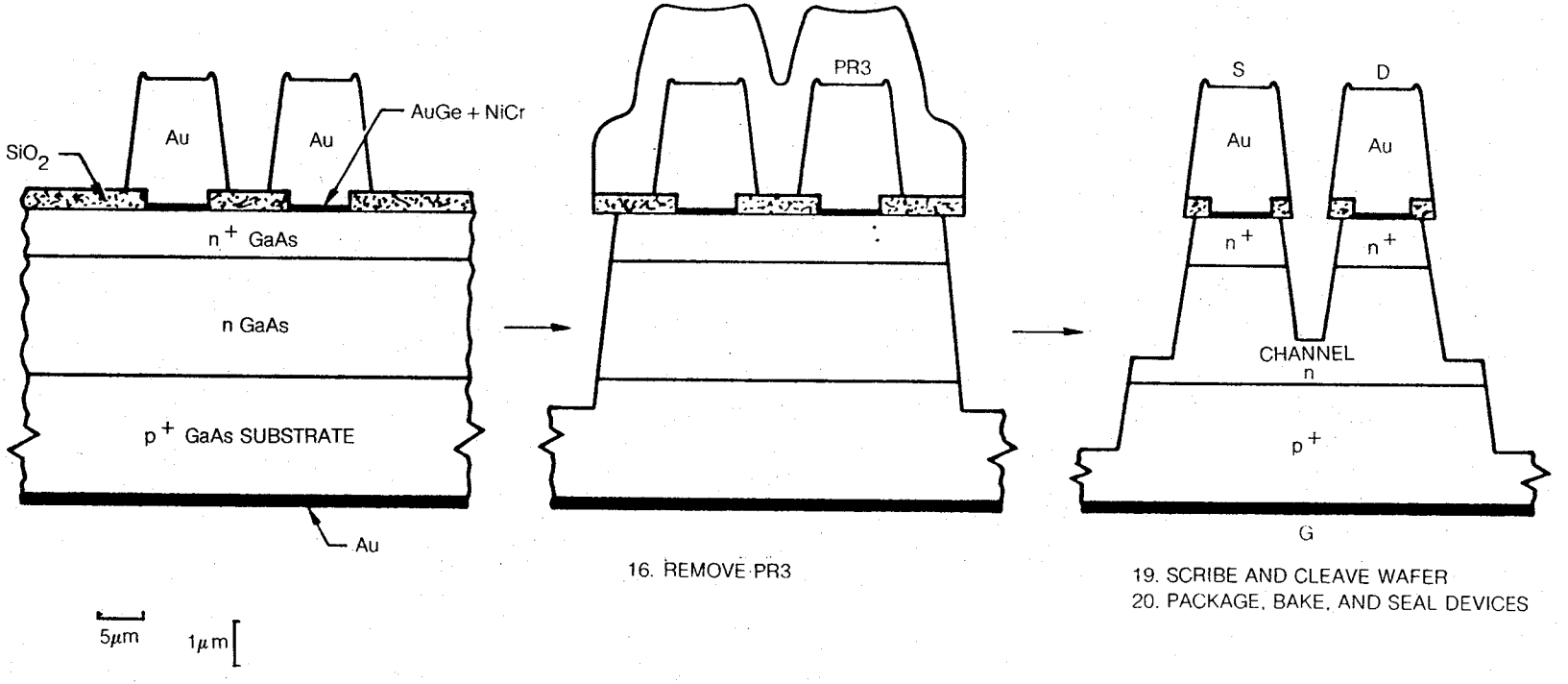
11. ION MILL Au AND PR2
12. REMOVE LEFTOVER PR2

DEVICE ISOLATION

13. PR DEVICE MESA (PR3)
14. ETCH SiO_2 BETWEEN DEVICES
15. ETCH GaAs BETWEEN DEVICES

CHANNEL FORMATION

17. ETCH SiO_2
18. ETCH GaAs CHANNEL



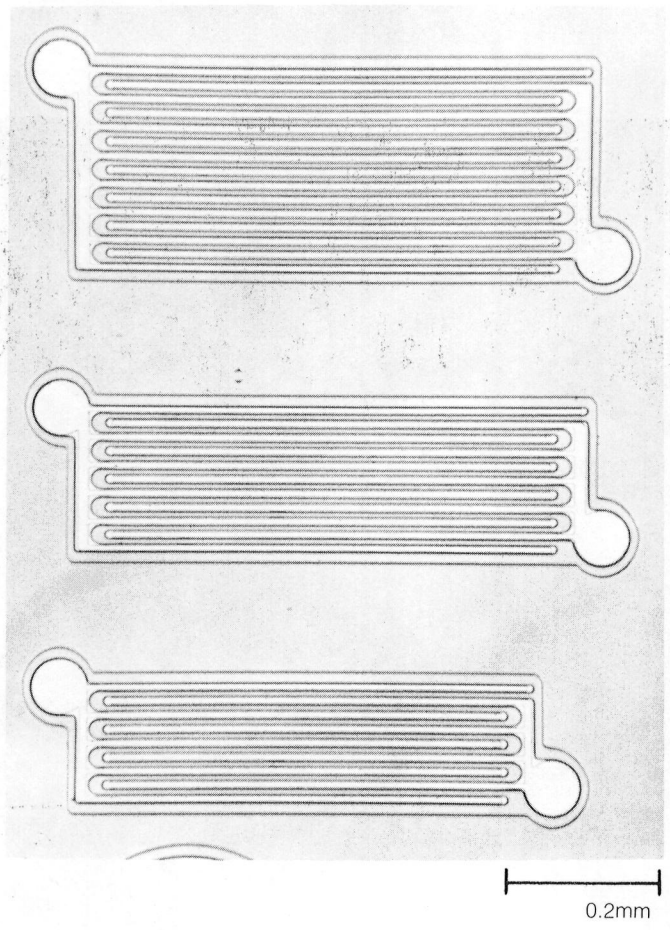
16. REMOVE PR3

19. SCRIBE AND CLEAVE WAFER
20. PACKAGE, BAKE, AND SEAL DEVICES

finger and bus build-up, finger formation, mesa isolation, and final channel formation. The process steps were very similar to those in phototransistor fabrication except that a channel had to be etched into the GaAs between source and drain and no anti-reflection coating was necessary. The quartz was used as a gold ion-mill stop and also to protect the AuGe-GaAs interface from possible lateral attack during GaAs etching. It was found important to remove the quartz at Steps 14 and 17 with plasma rather than wet chemical (BHF) etching in order to reduce quartz undercutting and enhance the effectiveness of the protection ridge. Figure 4-11 shows the three devices just before channel etching. The outer boundary line of each device was the mesa edge. The GaAs channel etching was carried out in stepwise fashion using $NH_4OH:H_2O_2:H_2O$ etches. Electrical measurements of the pitch-off voltage of sample JFET's were taken in between channel etchings. At each stage, devices whose pinch-off voltages had been trimmed into the acceptable range, were masked with wax from further etching. A cross-sectional view of JFET fingers and etched channel is shown in Fig. 4-12 for one GaAs chip which was cleaved parallel to the long direction of the chip. The channel length for this case was less than 0.5 μm. Channel length decreased with increasing etch depth and was strongly dependent on initial separation between gold fingers. Although not delineated, n-type GaAs material about one-micron thick did exist at the bottom of the "V". The photograph shows some expected undercutting of the metallization and quartz ridge material but not enough to cause metallization lifting. The step at the left side of Fig. 4-12 was the boundary of n-type GaAs material for the device, i.e., mesa edge.

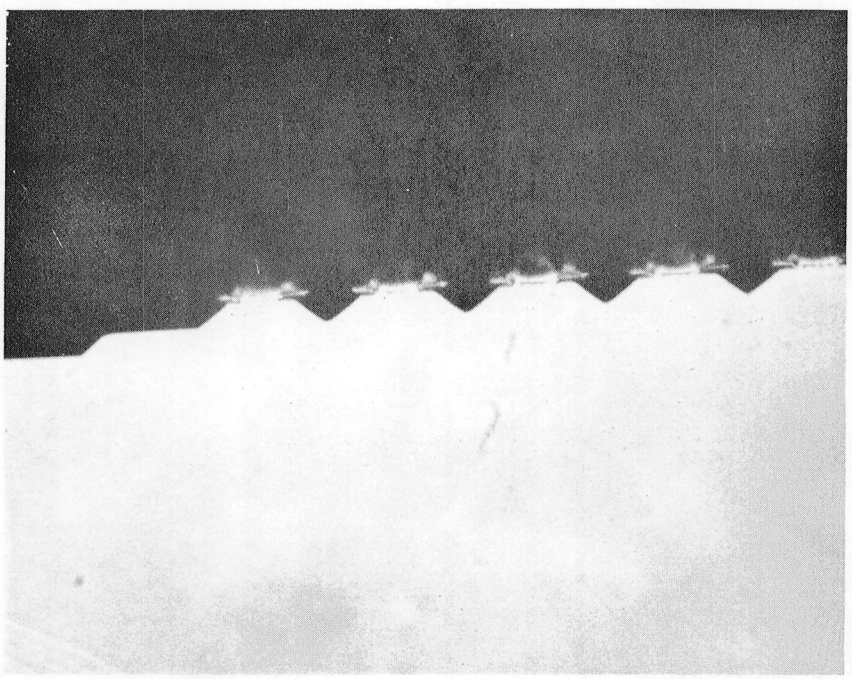
Figure 4-13 is a surface view of JFET's after channel etching, dicing, die bonding and thermocompression bonding with 25-μm-diameter gold wire. Some irregular surface lines, formed during channel etching along the wax boundaries are evident especially in the lower photograph. These do not affect device performance. Several important parameters that affected the required channel etch time for each device were the n^+ and n-epitaxial layer thickness, carrier concentration in the n layer, and finger separation. Variations in the values of these parameters across the wafer dictated the need for a gate trimming process. As an example of the thickness control required to produce across the entire wafer, a range of pinch-off voltages of -12V ± 1V (all other factors ignored), the n-type epitaxial layer thickness could not vary by more than ±0.05 μm from the required thickness of 2.5 μm for $n = 1 \times 10^{16} cm^{-3}$. On the other hand, if carrier concentration were the only variable, then n could not vary by more than $\pm 0.08 \times 10^{16} cm^{-3}$.

ON-WAFER GaAs JFETs PRIOR TO CHANNEL ETCHING



81–12–13–1

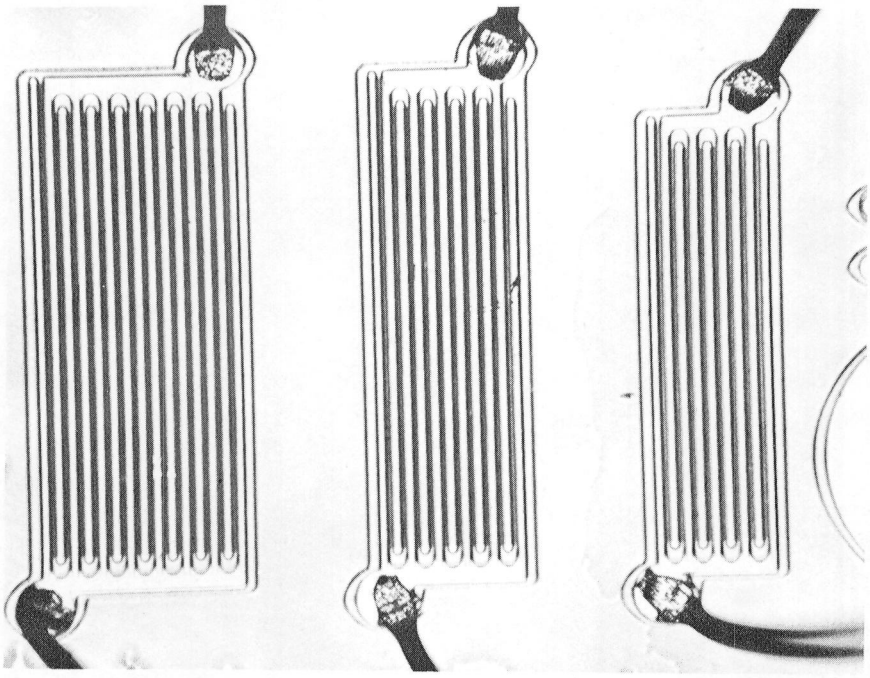
CROSS SECTIONAL VIEW OF JFET FINGERS



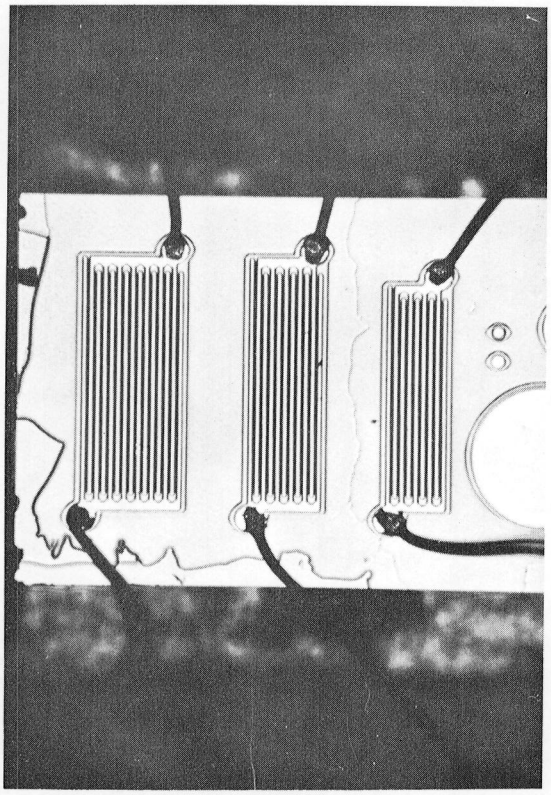
81-12-13-4

FIG. 4-13

GaAs JFETs AFTER WIRE BONDING



0.2mm



0.4mm

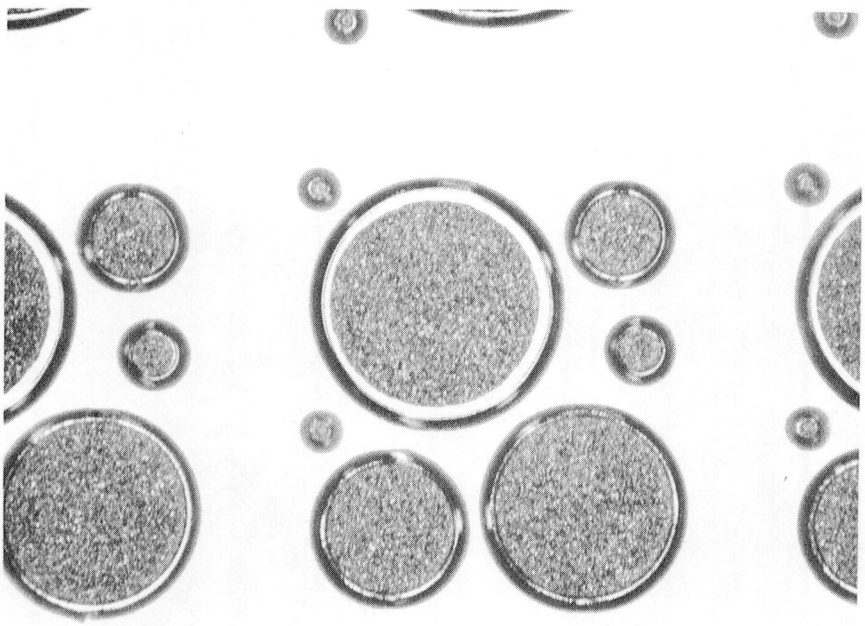
81–12–13–2

The GaAs transient-protection diodes were circular mesas with diameters of 76 μm to 320 μm. The process headings were contact definition, ohmic contact metallization, gold build-up on the mesa, gold mesa definition, and mesa isolation. For the anticipated switching transients and pulse-width modulation frequencies, a mesa diode structure having a 250-μm diameter or less, was required. Figure 4-14 shows finished on-wafer devices after mesa etching. Devices cut from this wafer were die bonded and the three intermediate-size diodes were wired into TO-5 packages (the two smallest structures on the chip were alignment circles).

Prior to hermetic sealing in a nitrogen ambient, the mounted and wired JFETs and diodes were vacuum baked at 200°C for about one hour. Selection of one JFET and one mesa diode per package for delivery in this program was based on electrical measurements described in the next section.

FIG. 4-14

GaAs TRANSIENT PROTECTION DIODES
(ON WAFER)



81–3–40–1

5.0 ELECTRICAL TESTING AND SELECTION OF GaAs PHOTOSWITCH DEVICES

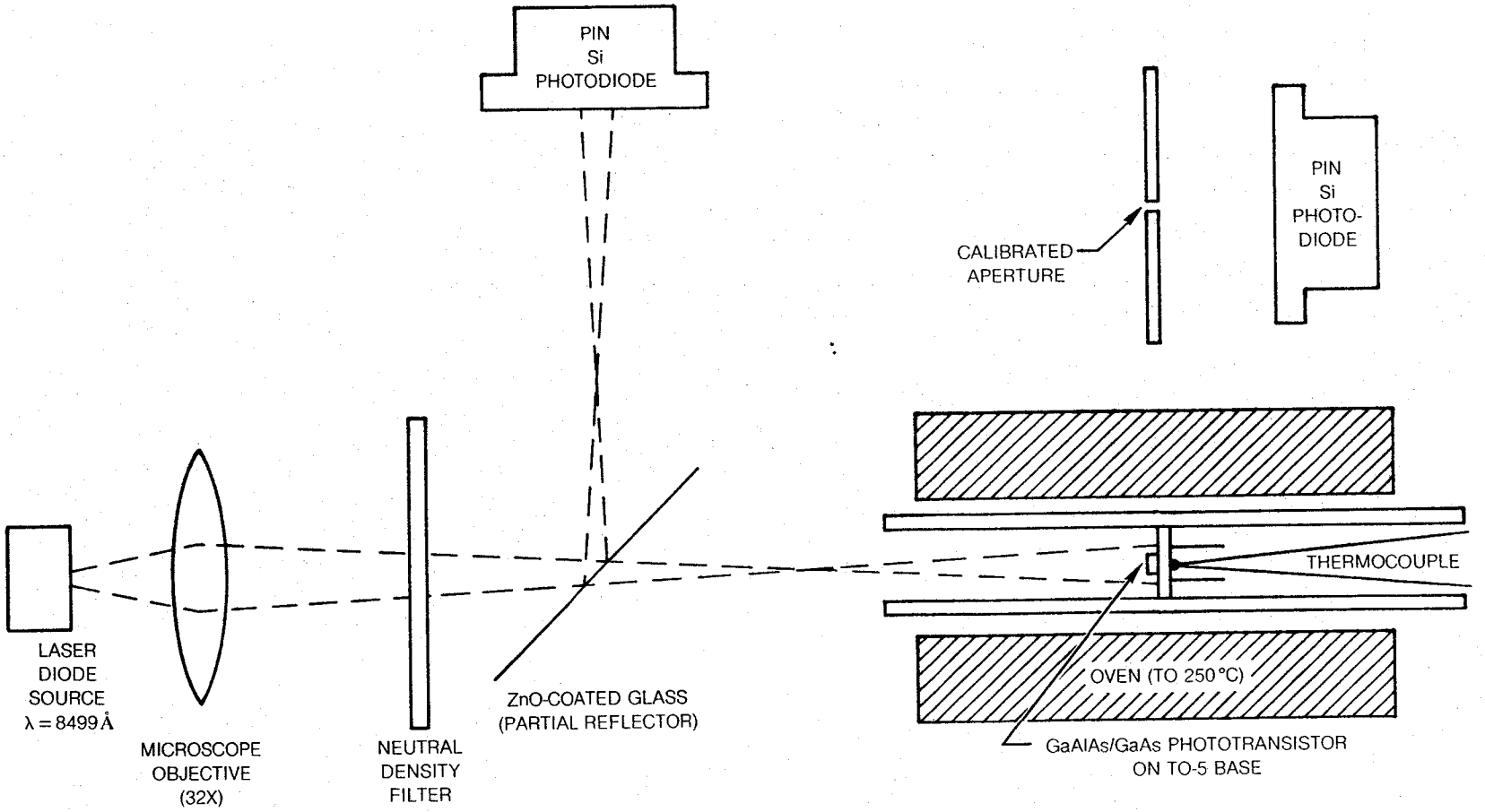
Selection of individual GaAs devices for use on the breadboard was based on a series of electrical testing at room temperature, 250°C, 175°C and -54°C and visual inspection for device or packaging defects. The screening procedure began with on-wafer electrical probing at room temperature. A device passing electrical tests and visual inspection was cleaved from the source wafer, mounted in a TO-5 package and thermocompression wire bonded with 25-μm-diameter wire. After further electrical tests, GaAs JFET's and diodes were hermetically sealed and subjected to electrical testing over the full temperature range. The three best JFET's and diodes were selected for breadboard testing. A full series of photoresponse measurements were conducted at room temperature, 175°C and 250°C on selected phototransistors mounted in TO-5 packages (not yet sealed). This was done to confirm phototransistor suitability for breadboard delivery prior to undertaking the difficult fiber sealing process. After hermetic sealing, phototransistors were again individually tested between -54°C and 250°C using IRED activation through the fiber optic pigtail, and three devices were passed to breadboard system testing which will be described in Section 6.0

5.1 Phototransistor Testing

Phototransistor requirements were that optical gain be high enough for activation by an IRED and dark current at 250°C be as low as possible. From Fig. 3-10 an experimental optical power density of about 1.6W/cm^2 can be provided at a phototransistor if placed 100 μm away from the optical fiber. For a 200-μm-diameter phototransistor, this corresponds to about 500 μW of incident optical power. Based on expected JFET offstate gate current and phototransistor dark current at 250°C, an expected value for R_s for the Case-II circuit in Fig. 3-3 was 10K ohms; therefore, about 1 to 1.4 mA of current flow in the phototransistor would be required to switch the JFET on. The phototransistor demand curves of Fig. 3-10 suggest that 500 μW is more than adequate for a phototransistor diameter of 200 μm for devices fabricated before this program began. However, this fact had to be checked for devices fabricated during this program before hermetic sealing with the fiber optic pigtail.

The experimental setup for photoresponse measurements on phototransistors mounted in TO-5 packages is shown in Fig. 5-1. Near-infrared cw laser diode radiation (wavelength = 8499Å) was brought to a focus in front of the phototransistor using a microscope objective. This was done in order to obtain a more uniform incident optical intensity across the device. A ZnO-coated-glass

EXPERIMENTAL ARRANGEMENT FOR HIGH-TEMPERATURE PHOTOTRANSISTOR TESTING BEFORE HERMETIC SEALING



81-8-11-12

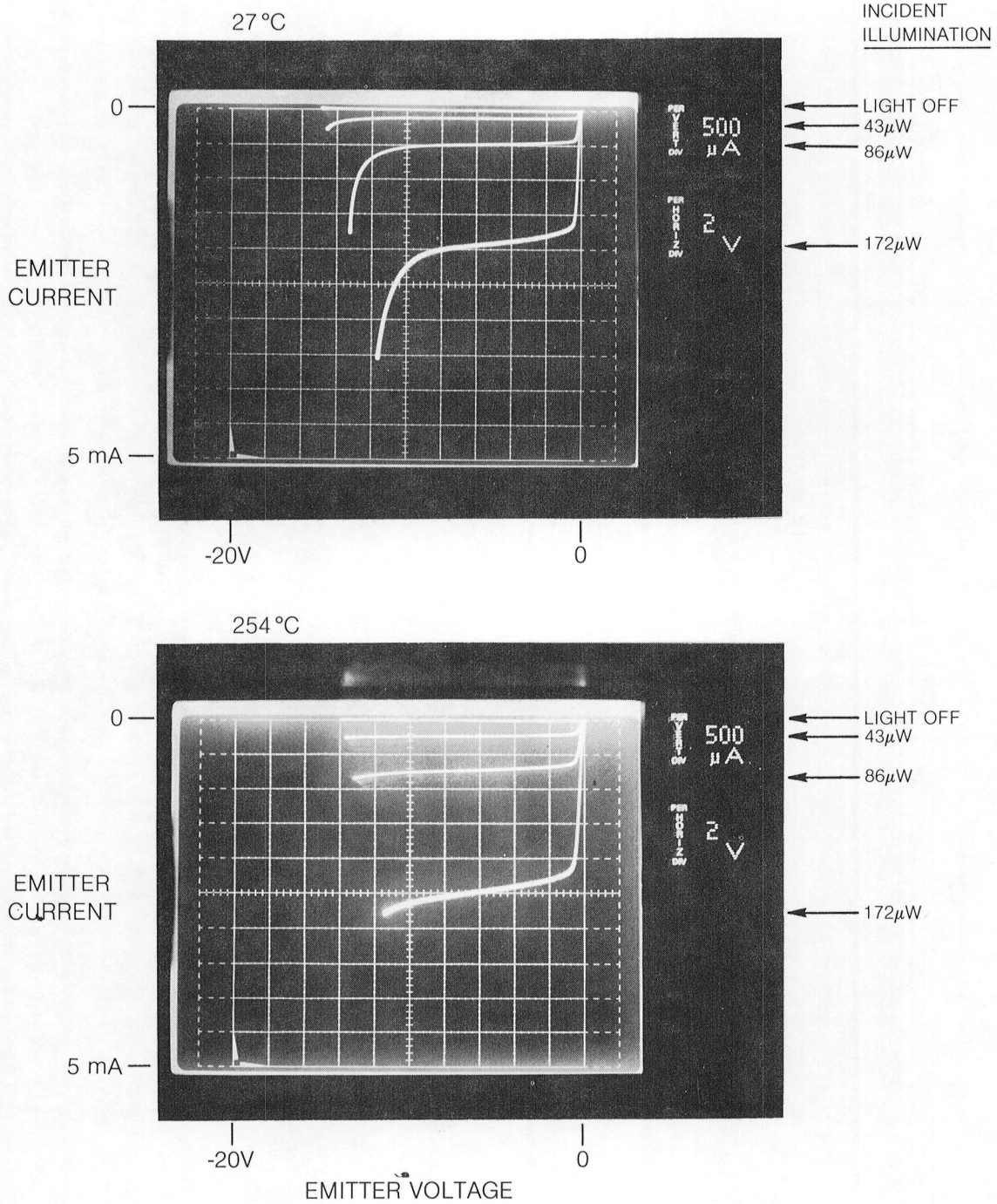
FIG. 5-1

reflector split part of the beam to a reference photodiode, the output of which was used to adjust the electrical power to the laser diode prior to each measurement. The optical power at the phototransistor was changed either by adding neutral density filters before the glass reflector or by changing the laser diode current. Prior to the phototransistor measurements, calibration of the incident radiation on the active surface area of the phototransistor was made at each laser diode current level using a 200-μm-diameter aperture which closely matched the phototransistor diameter. The aperture could be lowered into the position formerly occupied by the phototransistor. By recording the maximum amount of radiation passing through the aperture to a calibrated photodiode, the reference detector could be calibrated directly in terms of optical power incident on the phototransistor. The photogenerated currents were obtained by adjusting the phototransistor in the plane perpendicular to the beam direction to give a maximum response on the curve tracer. In a typical series of measurements optical response and dark current were measured near room temperature, 175°C and 250°C. After about a one-half to one-hour stabilization period at 250°C, another set of photoresponse measurements was taken near 250°C and then on cooling. A thermocouple, tack welded to the base, was used to monitor device ambient temperature inside a miniature oven.

Photoresponse measurements were made on twelve candidate phototransistors. Figures 5-2 through 5-5 show current-voltage curves for four devices at various levels of incident illumination on cooling from 254°C to room temperature. (Devices 013a, K11d, and R14a were eventually packaged and delivered with the breadboard and are appropriately reviewed here. Device K12d exhibited the highest gain of the twelve devices tested.) Emphasis during the measurements was placed on obtaining current-voltage characteristics at the 1mA to 5mA levels. When used with the GaAs JFET switch, the phototransistor should supply photocurrent with minimal internal voltage drop; therefore, the current at the knee of each curve is the maximum allowable current. As can be seen, the knee voltage drop is one volt or less at these illumination levels. Actually, the knee emitter-collector voltage is closer to -0.4V to -0.5V for expected photocurrent levels. These voltages will also appear on the JFET gate (on-state) in the Case-II circuit configuration (Fig. 3-3). Figures 5-6 and 5-7 show phototransistor dark currents at 253°C. When used in the Case-II configuration, the phototransistor is reversed biased at -10 to -14V when not illuminated. The value of dark current at the maximum operating temperature is an important parameter in determining the Case-II value of R_s. Smaller dark current allows use of a larger R_s, which draws smaller phototransistor operational current and requires less IRED optical power. The dark current per unit area for devices fabricated during this program was much less than for the devices measured during the design stage (Fig. 3-7). The design-stage phototransistors must have had surface or defect

PHOTOTRANSISTOR CURRENT-VOLTAGE CHARACTERISTICS (O13a)

BASE FLOATING-COLLECTOR GROUNDED
$\lambda = 8499 Å$

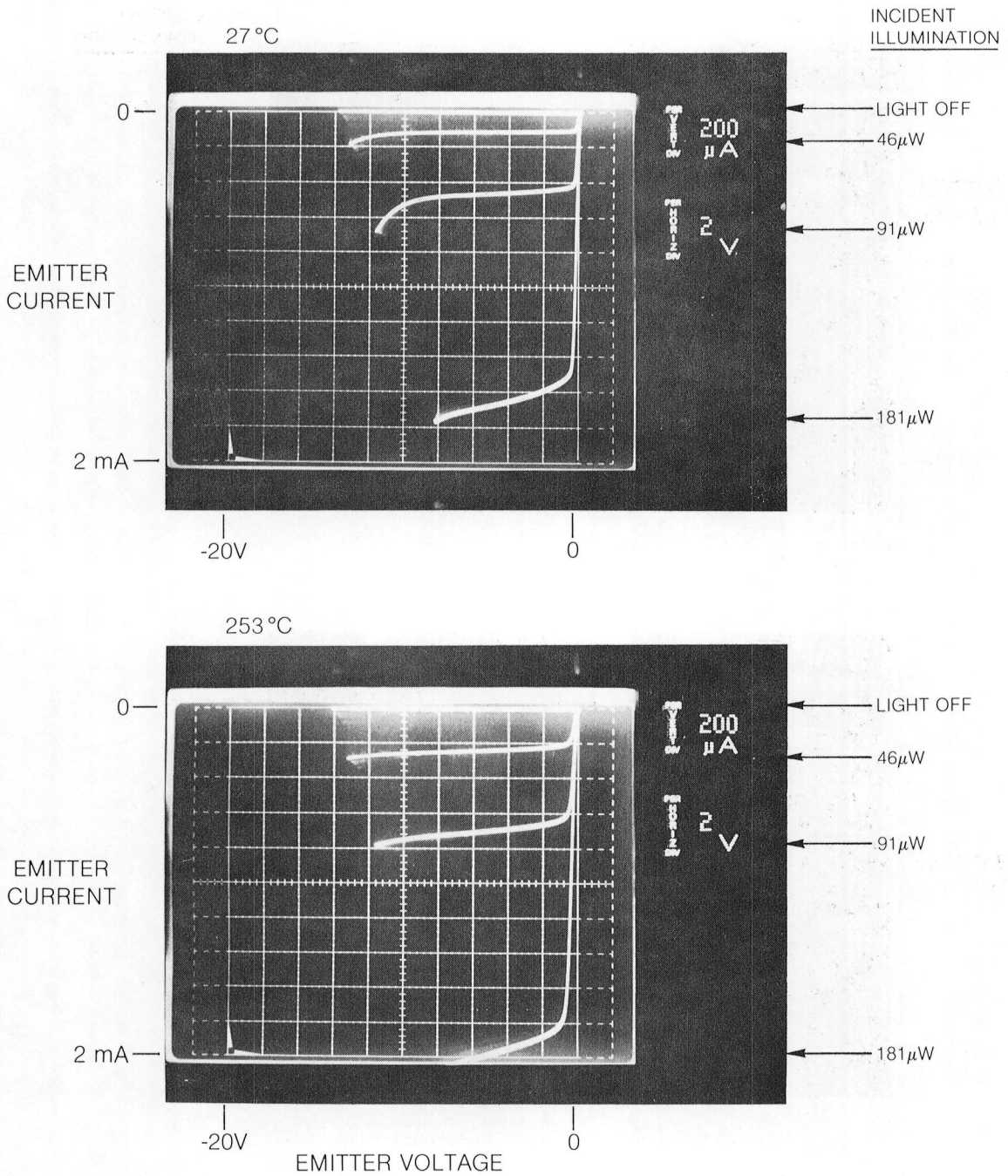


81–8–11–1

PHOTOTRANSISTOR CURRENT-VOLTAGE CHARACTERISTICS (K11d)

BASE FLOATING-COLLECTOR GROUNDED

$\lambda = 8499\text{Å}$

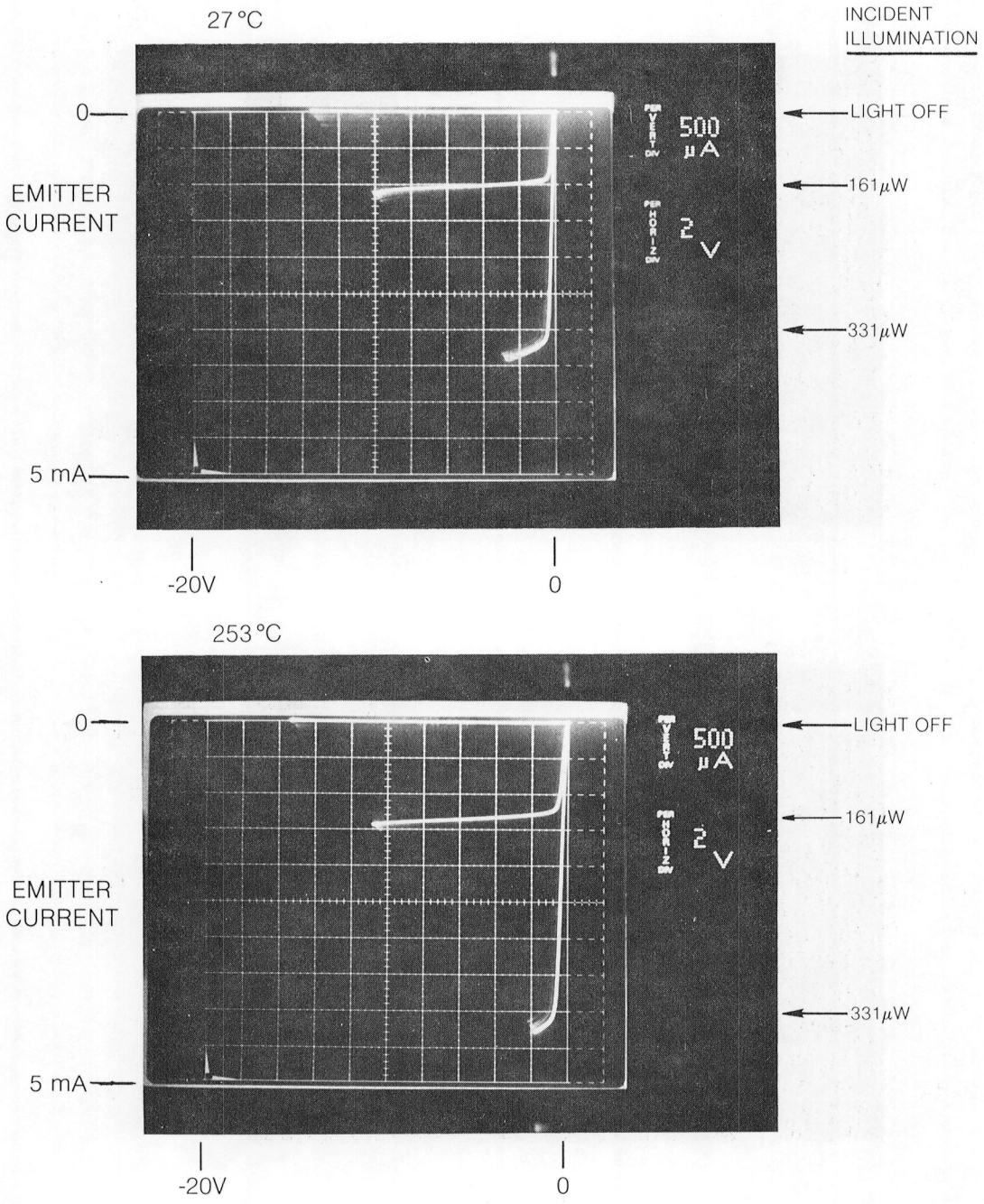


83-3-119-7

PHOTOTRANSISTOR CURRENT-VOLTAGE CHARACTERISTICS (R14a)

BASE FLOATING-COLLECTOR GROUNDED

$\lambda = 8499\text{Å}$

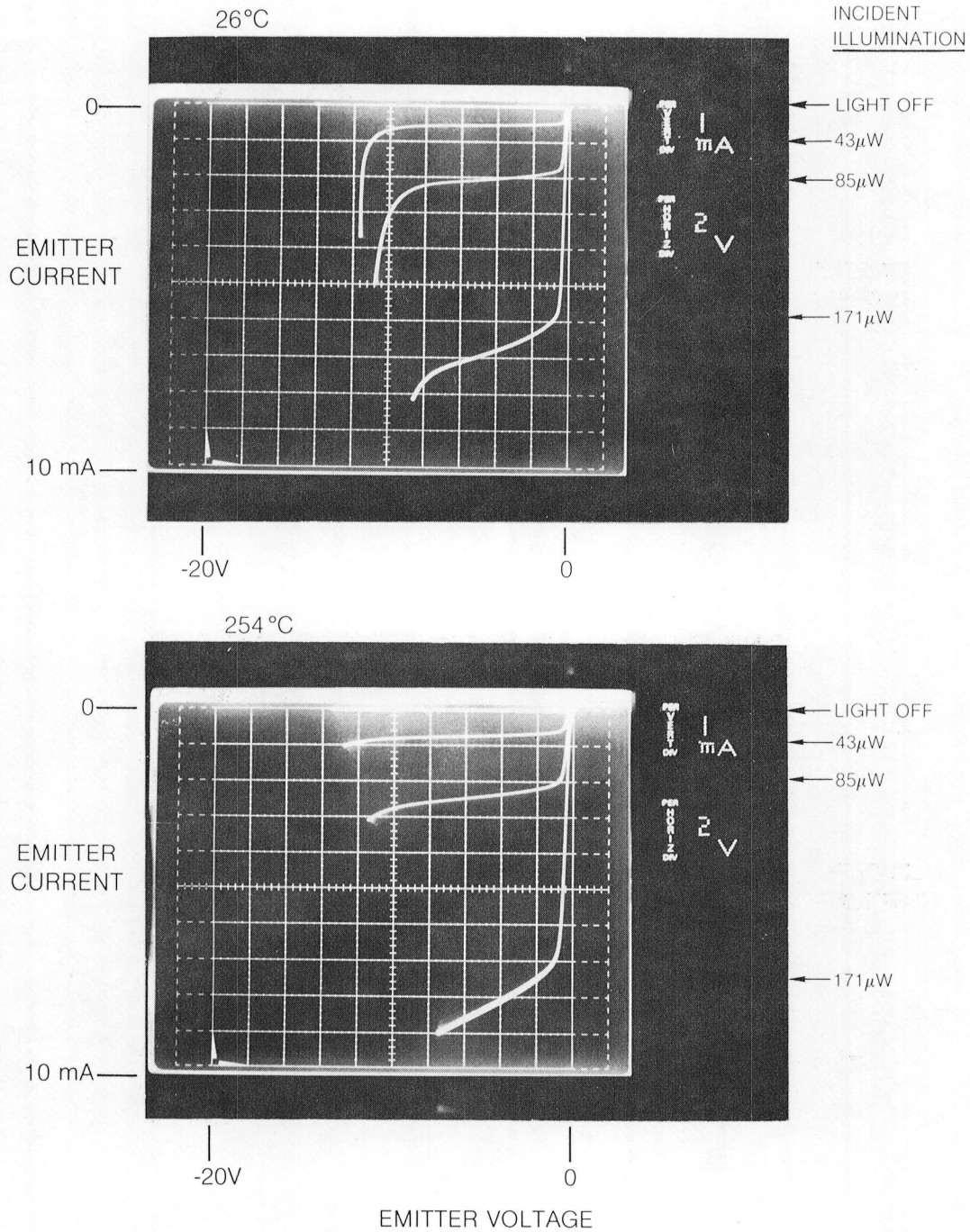


83–3–119–8

PHOTOTRANSISTOR CURRENT-VOLTAGE CHARACTERISTICS (K12d)

BASE FLOATING-COLLECTOR GROUNDED

$\lambda = 8499\text{Å}$

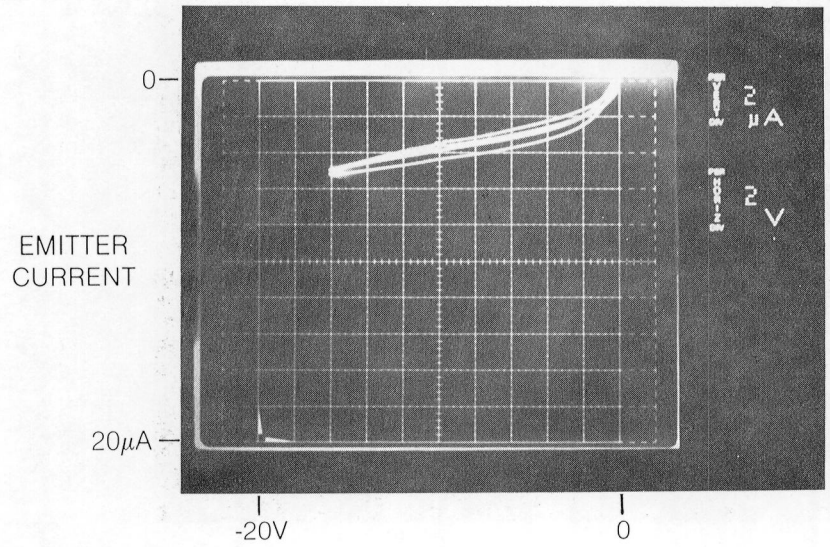


83–3–119–9

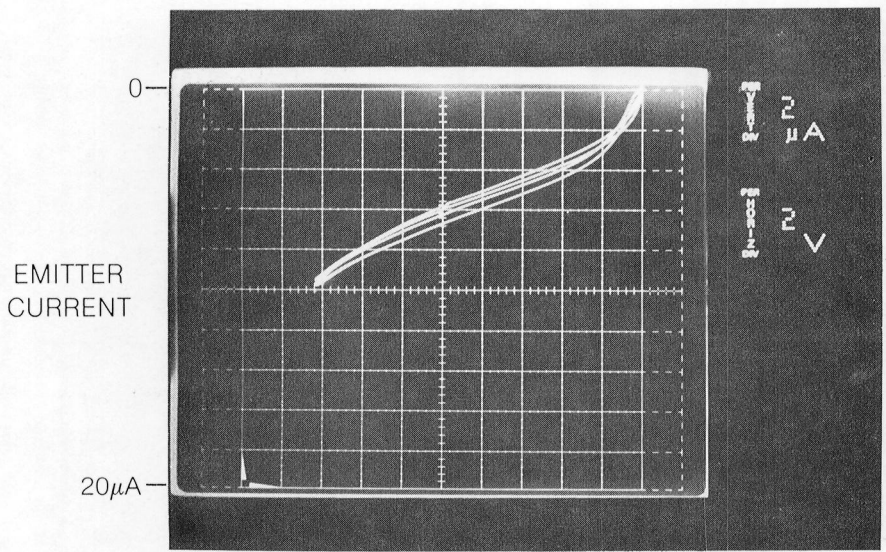
FIG. 5-6

PHOTOTRANSISTOR DARK CURRENT AT 253°C

DEVICE O13a



DEVICE K11d

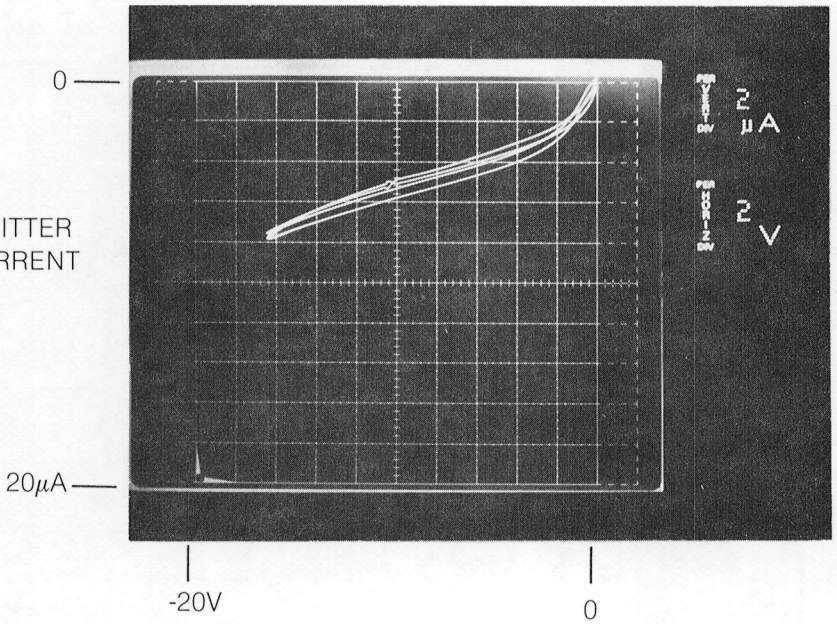


83-3-119-10

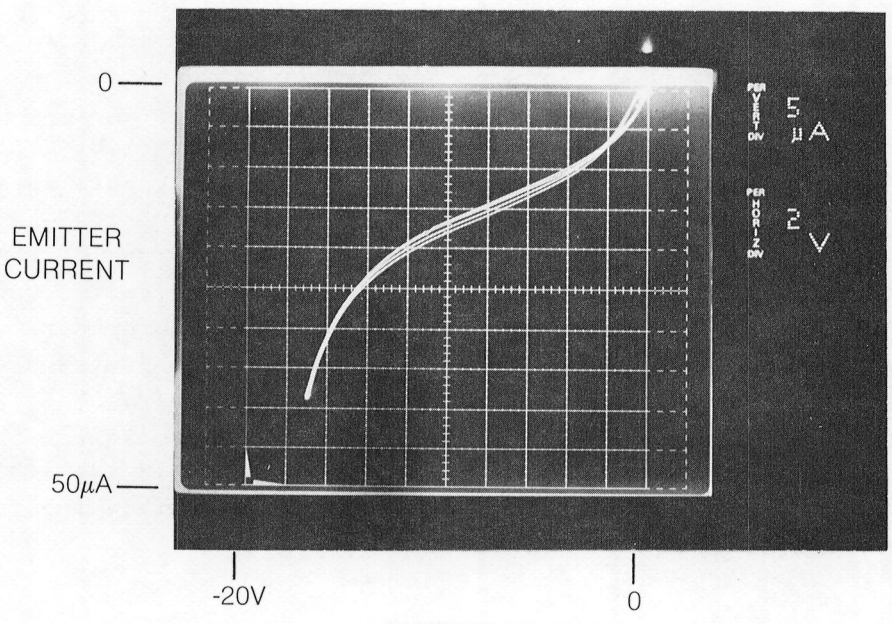
FIG. 5-7

PHOTOTRANSISTOR DARK CURRENT AT 253°C (CONTINUED)

DEVICE R14a



DEVICE K12d



83-3-119-11

currents flowing along with the ordinary junction current. The dark currents at 175°C for the program phototransistors were not measurable on the curve tracer, i.e., under 200 nA. The important conclusion from Figs. 5-2 through 5-7 is that sufficient optical power is available from the IRED to operate the photoswitch system with the phototransistor placed in the Case-II configuration and for expected values of JFET maximum off-state gate current.

A summary of calculated knee optical gains at two illumination levels and dark current at -12V and 250°C is given in Table VII for all twelve phototransistors. The optical gain is defined as the current measured at the knee of the current-voltage curve divided by current calculated from the infrared exposure (Eq. 3-5). A small correction (less than 8%) to the knee current at 250°C due to device dark current at the knee voltage was made at the 18 μm exposure level shown in the table. For each device the measurements were divided into two sets separated by a stabilization period during which generated photocurrents (and optical gains) were observed to increase with time at 250°C. About one-half to one hour was required for stabilization of the photocurrents. When measurements were repeated at 250°C and at lower temperatures, all devices showed improved gains, the effect being largest for the room temperature values. In one case, device K13d, the measurements were repeated the following day and the improved gains were still observed. The suspected reason for the optical gain increases was annealing of defects at the heterojunction interface which then increased the injection efficiency and device gain. Some other observations supported by Table VII are: (1) Optical gain increases with optical illumination. This is commonly observed with heterojunction phototransistors. (2) After stabilization, the optical gain is generally highest at 250°C for both exposure levels. This was not always the case as evidenced by device G9d. The values near 175°C generally lay between values at 250°C and room temperature. (3) Dark current was not strongly affected during the measurements. Again, device G9d was a notable exception.

A summary of post-stabilization phototransistor data including calculated knee optical gains, measured knee photocurrents and dark currents is shown in Table VIII. The devices are listed in order of decreasing optical gain at the 170 μW illumination level and at 253°C. The optical gains ranged from 61 to 10.5 at 253°C compared to 51 to 8 at room temperature. The corresponding photocurrents are listed. The highest measured phototransistor dark current was for device K12D. It is expected that the higher-gain phototransistors should display higher dark currents since the thermally generated carriers, as with photogenerated carriers, will be amplified by the phototransistor. This trend is generally supported by the measured dark currents in the last column of this table; however, the presence of highly variable surface and defect leakage currents complicates the analysis.

TABLE VII

PHOTOTRANSISTOR DATA PRIOR TO HERMETIC SEALING

Optical Gain and Dark Current

Device	Temperature (°C)	Optical Gain At Knee At 170 μW	Optical Gain At Knee at 18 μW	Dark Current at -12V (μA)
K13d	26	14.3	0.7	--
	175	16.2	1.5	--
	252	16.6	2.2	5
	Stabilize			
	252	17.5	2.4	4.5
	179	19.6	1.6	--
	28	20	1.0	--
	26 (Next Day)	21	0.8	--
	252 (Next Day)	18.4	2.5	4
	30 (Next Day)	21	0.8	--
013a	26	10	0.8	--
	176	14.1	2.0	--
	251	17.4	3.4	4.4 (253°C)
	Stabilize			
	254	18.7	3.5	--
	179	18.3	2.4	--
	27	14.4	1.1	--
J10d	27	11.3	1.3	--
	178	16.2	2.7	--
	253	21	4.5	13
	Stabilize			
	254	25	6.1	15 (253°C)
	178	23.2	3.9	--
	27	19.4	1.6	--
G13b	26	30	3.1	--
	179	35	5.4	--
	253	40	6.6	9 (254°C)
	Stabilize			
	254	43	7.9	12
	180	42	6.1	--
	27	37	4.0	--

TABLE VII (Continued)

PHOTOTRANSISTOR DATA PRIOR TO HERMETIC SEALING

Device	Temperature (°C)	Optical Gain At Knee At 170 μW	Optical Gain At Knee At 18 μW	Dark Current at -12V (μA)
K11d	25	6.4	1.0	---
	178	10.3	2.3	---
	254	12.4	3.4	7 (253°C)
	Stabilize			
	253	14.8	3.7	7
	179	15.8	3.2	---
	27	12.1	1.1	---
R14a	26	5.8	0.9	---
	178	7.9	1.8	---
	252	8.5	2.3	5.5 (253°C)
	Stabilize			
	253	10.5	2.8	6
	176	10.2	1.9	---
	27	8	1.2	---
F13b	25	9.3	1.1	---
	179	12.2	2.0	---
	252	13.6	2.8	6.6 (253°C)
	Stabilize			
	253	14.2	3.3	7
	176	14.1	2.0	---
	27	11	1.2	---
K12d	25	30	3.9	---
	177	42	6.2	---
	251	56	11.8	16
	Stabilize			
	254	61	12.8	20 (253°C)
	179	58	9.9	---
	26	51	5.4	---

TABLE VII (Continued)

PHOTOTRANSISTOR DATA PRIOR TO HERMETIC SEALING

Device	Temperature (°C)	Optical Gain At Knee		Dark Current at -12V (μA)
		At 170 μW	At 18 μW	
K5b	27	20	1.8	---
	177	28	3.4	---
	253	35	5.2	17
	Stabilize			
	253	43	5.9	13
	177	41	4.4	---
	27	34	2.1	---
G9d	27	9.6	2.0	---
	177	10.5	2.1	---
	252	11	2.6	4.0 (253°C)
	Stabilize			
	253	12.4	3.2	8.5
	177	14.5	2.9	---
	27	16.2	2.8	---
K4d	26	7.3	0.9	---
	177	9.1	1.5	---
	253	10.7	2.1	3.4
	Stabilize			
	253	12.9	3.2	4.0
	177	13.3	2.1	---
	27	12.2	1.3	---
K6b	27	6.6	0.9	---
	177	8.5	1.5	---
	253	9.7	2.0	3.6
	Stabilize			
	253	11.3	2.6	4.2
	177	11.6	1.9	---
	27	9.8	1.1	---

TABLE VIII

POST-STABILIZATION PHOTOTRANSISTOR DATA

Device	T (°C)	Knee Optical Gain at 170 μW		Knee Photocurrent at 170 μW (mA)		Dark Current at -12V and 253°C (μA)	
K12d	254	61		7.1		20	
	26		51		6	--	
K5b	253	43		4.8		13	
	27		34		3.8	--	
G13b	254	43		5		12	
	27		37		4.3	--	
J10d	254	25		3		15	
	27		19.4		2.3	--	
013a	254	18.7		2.2		4.4*	
	27		14.4		1.7	--	
K13d	252	18.4		2.2		4	
	26		21		2.4	--	
K11d	253	14.8		1.8		7	
	27		12.1		1.5	--	
F13b	253	14.2		1.7		7	
	27		11		1.3	--	
K4d	253	12.9		1.5		4	
	27		12.2		1.4	--	
G9d	253	12.4		1.4		8.5	
	27		16.2		1.9	--	
K6b	253	11.3		1.3		4.2	
	27		9.8		1.1	--	
R14a	253	10.5		1.2		6	
	27		8		0.95	--	

*Before stabilization

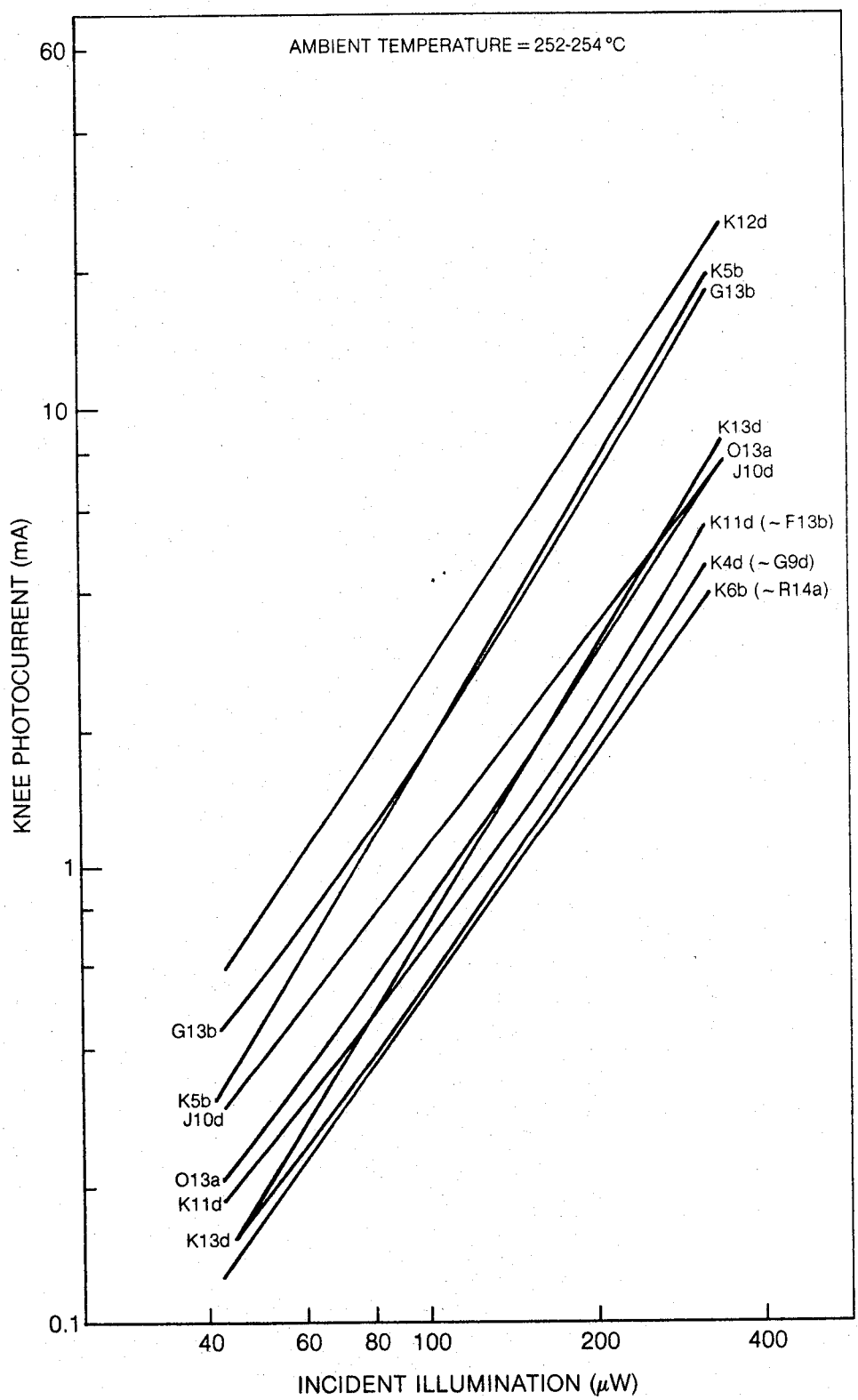
A complete summary of photocurrent and optical-gain data gathered during the post-stabilization period (and prior to hermetic sealing) at 250°C and at room temperature is shown in Figs. 5-8 through 5-11. These data illustrate trends previously mentioned and indicate the capability of any of the phototransistors for delivering up to 1.4 mA of photocurrent during breadboard operation using IRED optical activation.

After hermetic sealing to the cap assembly, each phototransistor was individually tested near -54°C, 25°C and 250°C. The first three packaged devices with adequate photoresponse and low dark current were reserved for breadboard testing in the photoswitch system. For the individual phototransistor testing, optical output from the breadboard IRED was coupled into the fiber-optic pigtail. For the measurement results that follow, the cited optical power values are an estimate of the infrared power emitted from the fiber inside the phototransistor package. The actual power striking the phototransistor was necessarily less due to the fiber numerical aperture and fiber separation from the phototransistor. The maximum fiber emission was 1.2 mW. Pertinent current-voltage characteristics for the three fully-packaged deliverable phototransistors are shown in Figs. 5-12 through 5-17. First of all, there is good agreement between the dark current curves and the respective curves prior to hermetic sealing (Figs. 5-6 and 5-7). Secondly, all the devices were capable of delivering much more than the 1.4-mA expected photocurrent for photoswitch operation using IRED activation.

In the same manner as before, the knee photocurrents from the current-voltage curves have been plotted as a function of optical power at the measured temperatures in Figs. 5-18 and 5-20. These are the three curves similarly labeled in each figure where the x-axis optical power is the estimated optical emission inside the package. For reference, the post-stabilization pre-hermetic-sealing photoresponse is also shown. Here the x-axis values represent actual laser diode power incident onto the phototransistor active area. The 250°C and room temperature curves track very well in each case. The x-axis displacement should correspond to optical losses associated with fiber-phototransistor coupling -- that is, NA loss or misalignment. The x-axis displacement would then correspond to the following coupling factor losses in optical power: (1) 013a - 1.4X (1.5 dB), (2) K11d - 1.3X (1.2 dB), (3) R14a - 2.2X (3.4 dB). These have to be regarded as minimum losses since the phototransistors were exposed to temperatures near 300°C in the final hermetic sealing. As a result some optical gain increases may have occurred similar to changes observed during earlier phototransistor measurements (Table VII). Due to observed differences in the photoresponse versus temperature, proper breadboard photoswitch operation is assured over the -54°C to 250°C range if the minimum required optical power is based on the curve near -54°C.

FIG. 5-8

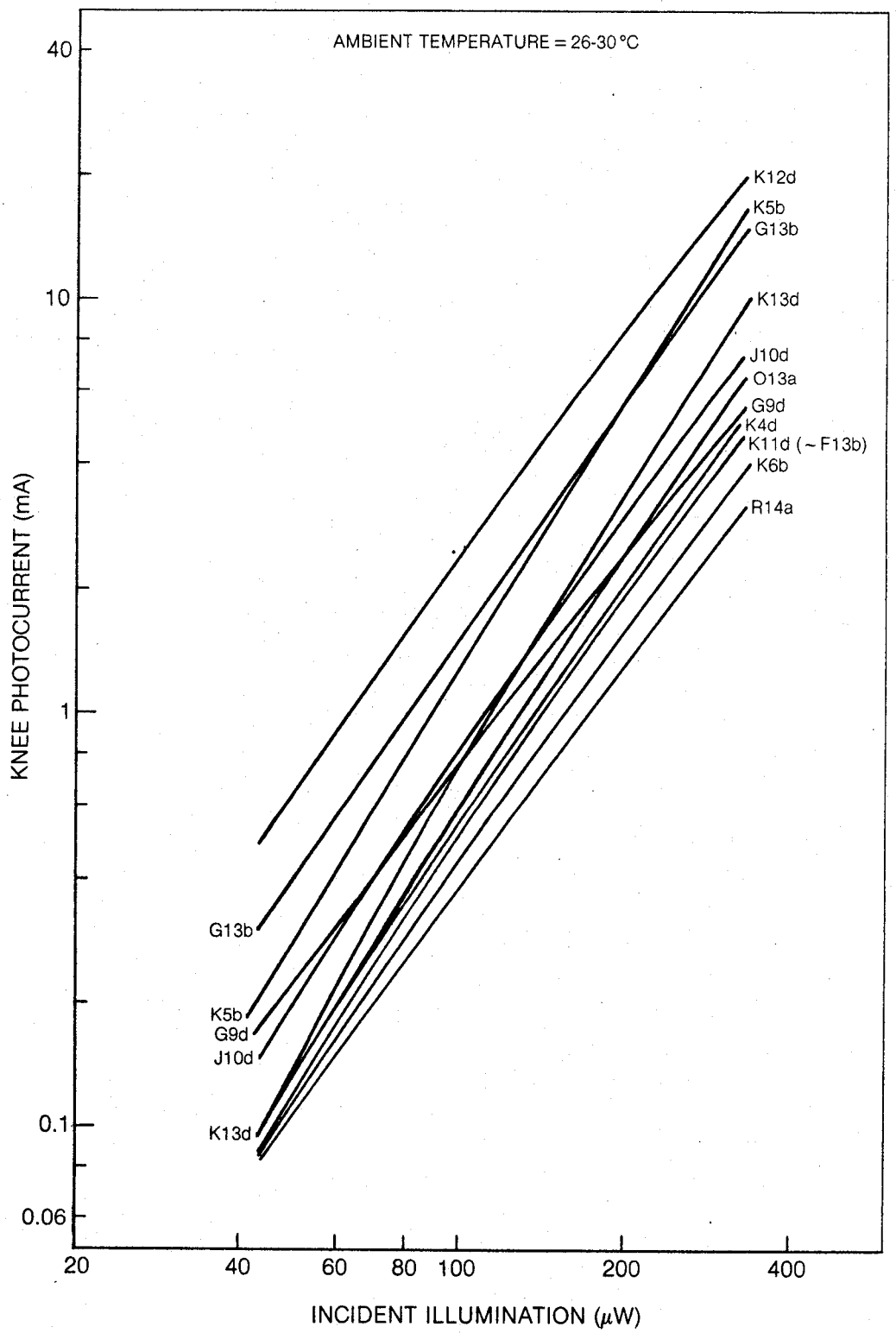
SUMMARY OF PHOTOTRANSISTOR PHOTORESPONSE NEAR 253°C



81–10–17–7

FIG. 5-9

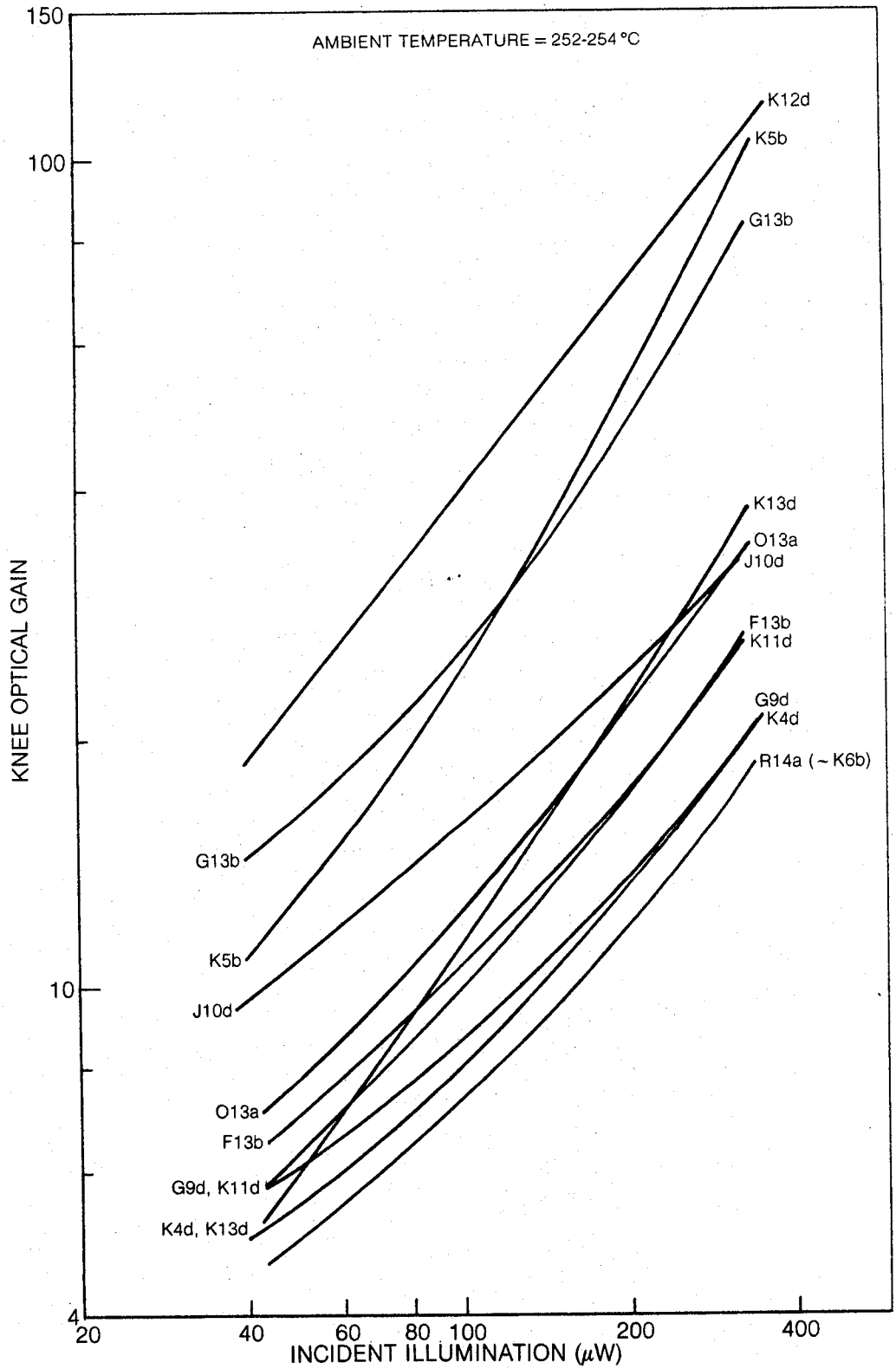
SUMMARY OF PHOTOTRANSISTOR PHOTORESPONSE AT ROOM TEMPERATURE



83-3-119-12

FIG. 5-10

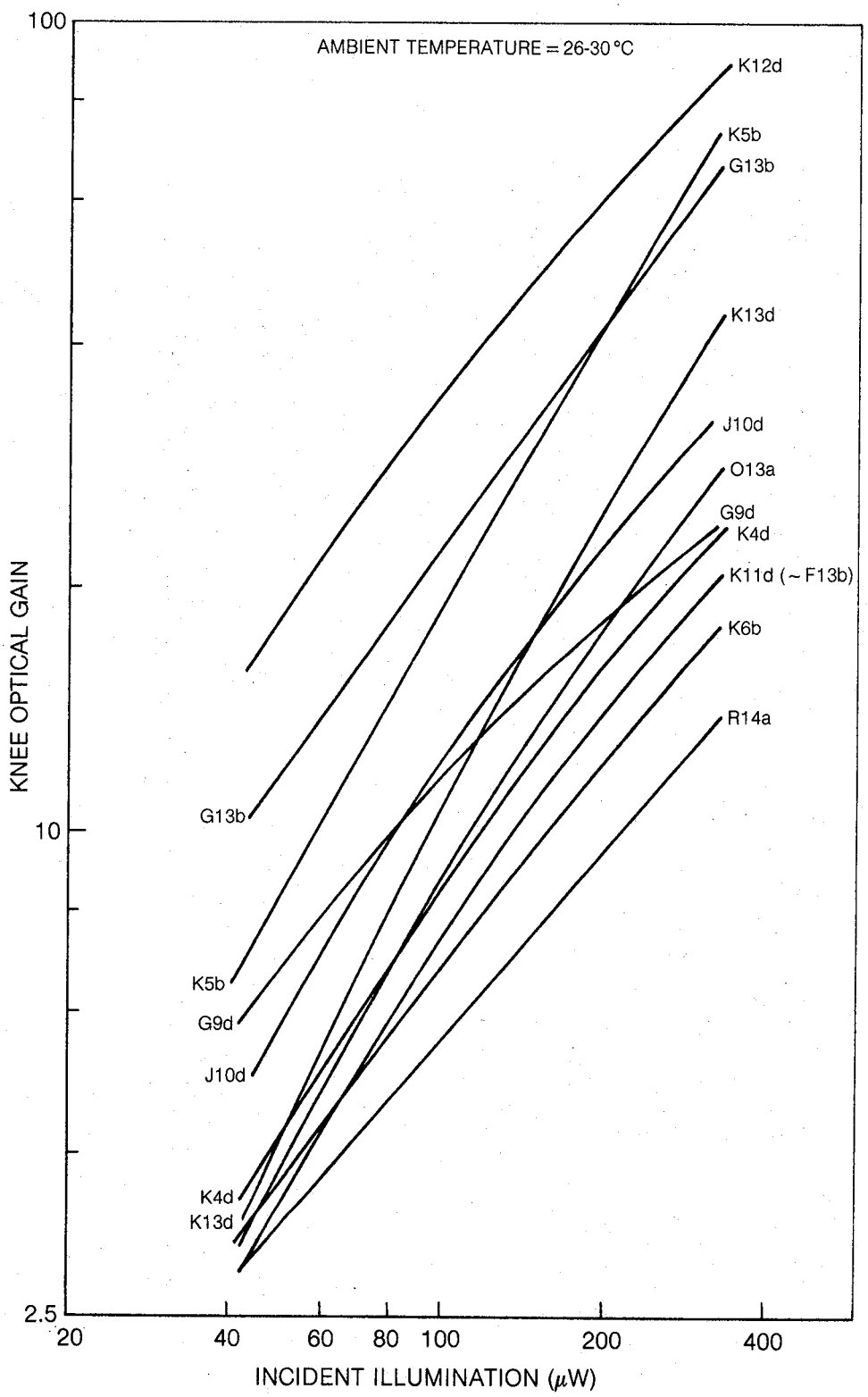
SUMMARY OF PHOTOTRANSISTOR OPTICAL GAIN NEAR 253°C



83-3-119-13

FIG. 5-11

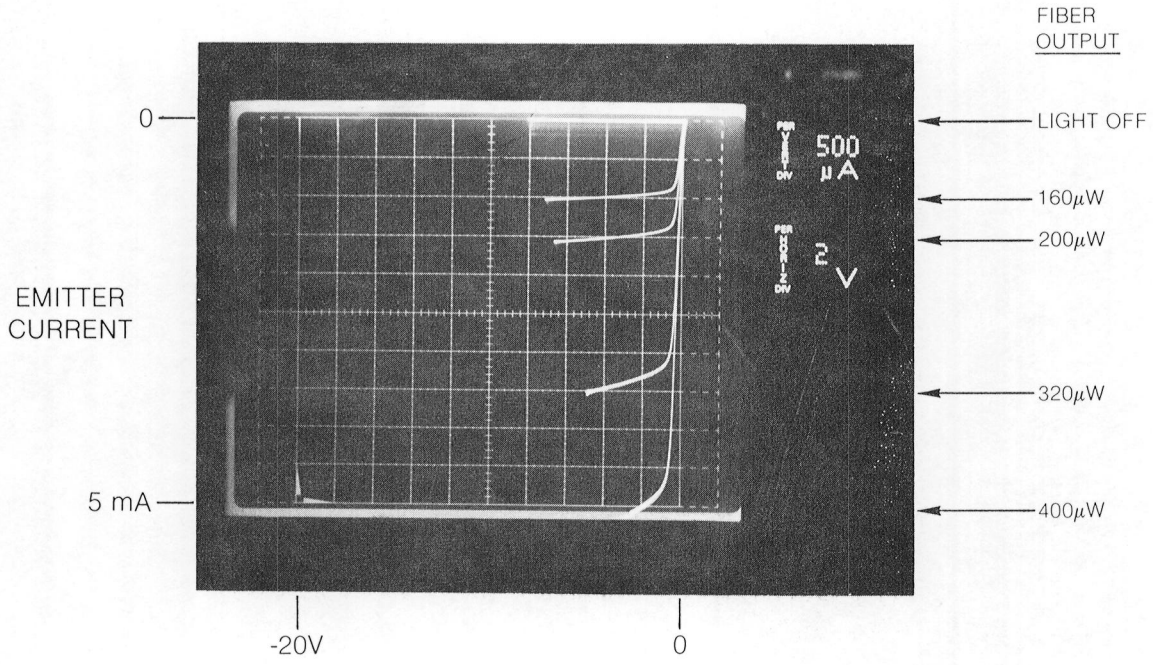
SUMMARY OF PHOTOTRANSISTOR OPTICAL GAIN AT ROOM TEMPERATURE



83-3-119-14

CURRENT-VOLTAGE CHARACTERISTICS AT 251°C FOR PHOTOTRANSISTOR O13a WITH f-o PIGTAIL

BASE FLOATING — COLLECTOR GROUNDED
$\lambda = 8360\text{Å}$ (BREADBOARD IRED)



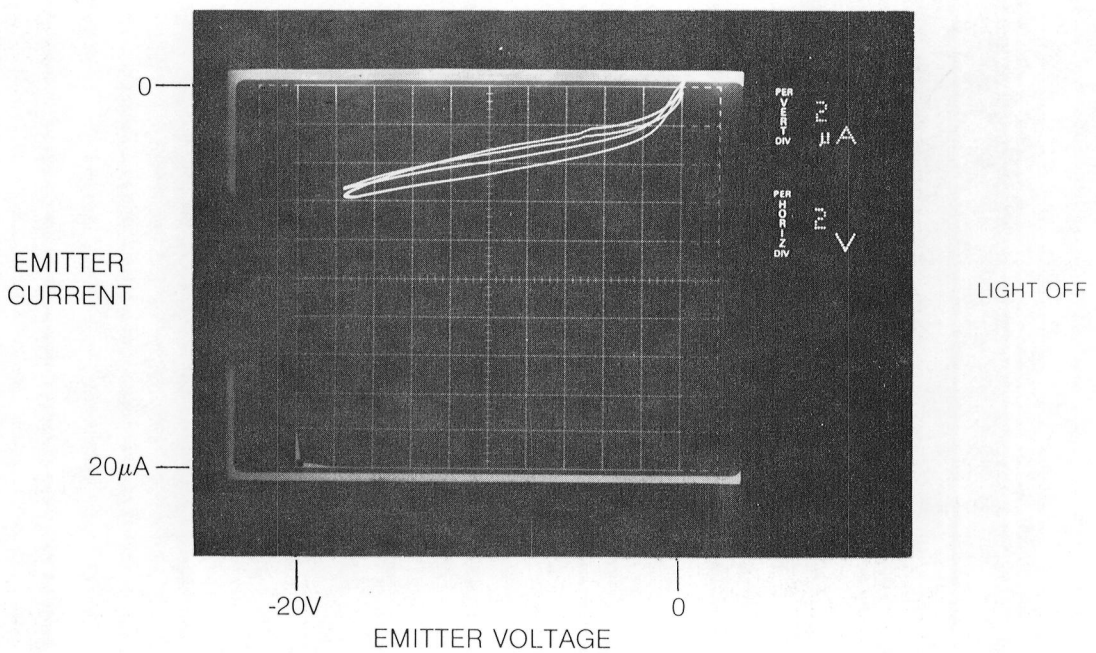
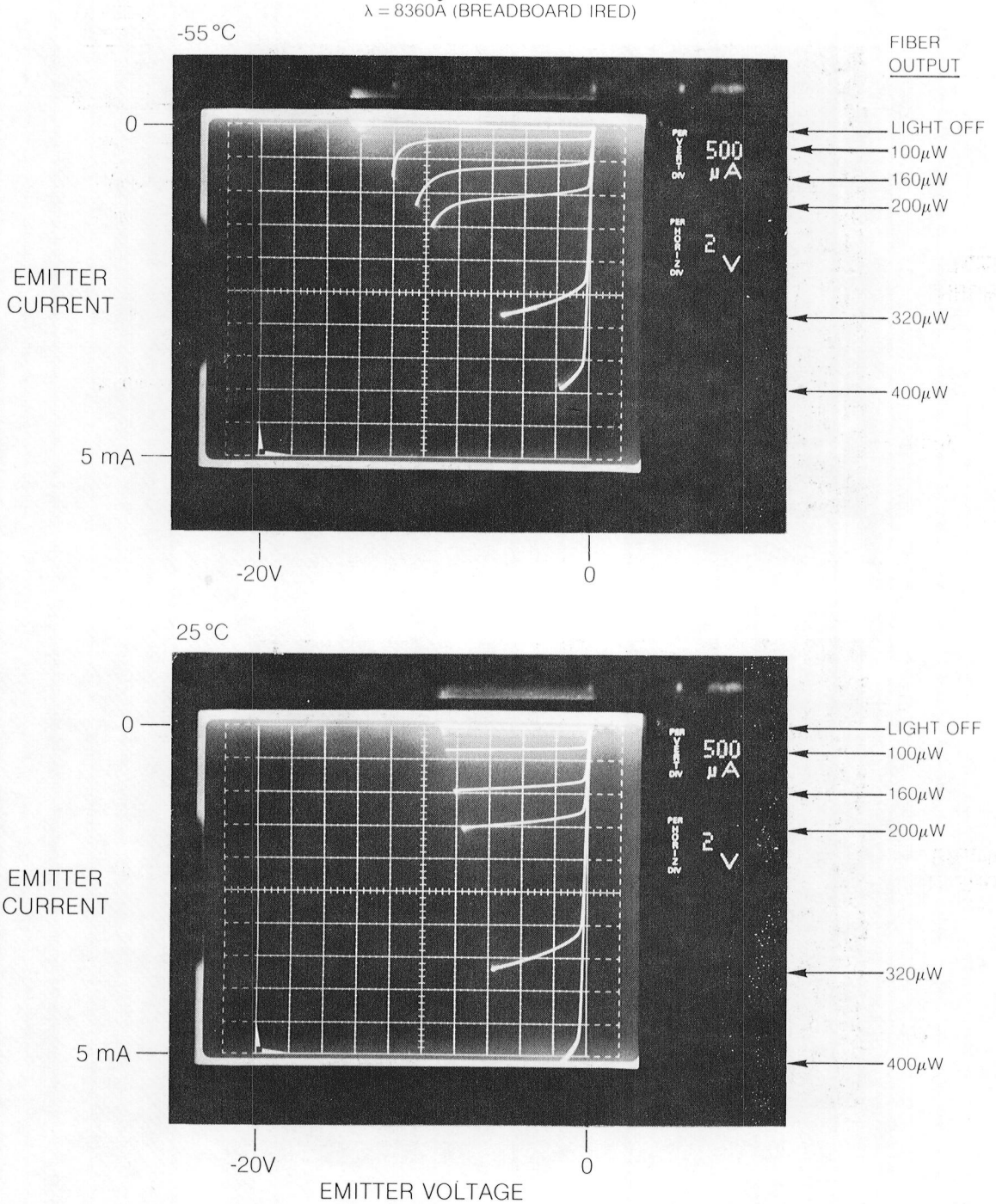


FIG. 5-13

CURRENT-VOLTAGE CHARACTERISTICS FOR PHOTOTRANSISTOR O13a WITH f-o PIGTAIL

BASE FLOATING — COLLECTOR GROUNDED

λ = 8360Å (BREADBOARD IRED)

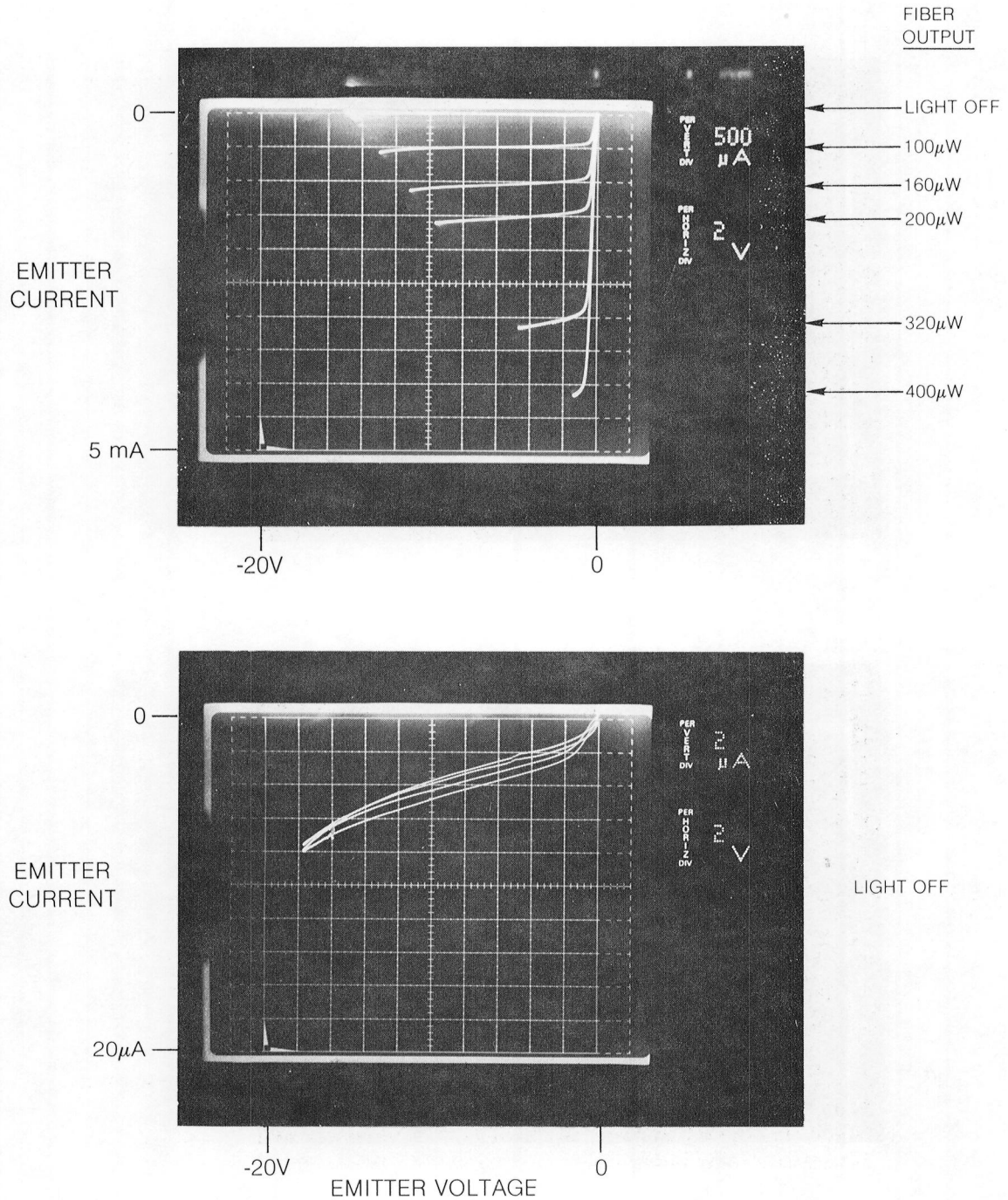


83-3-119-16

CURRENT-VOLTAGE CHARACTERISTICS AT 251°C FOR PHOTOTRANSISTOR K11d WITH f-o PIGTAIL

BASE FLOATING — COLLECTOR GROUNDED

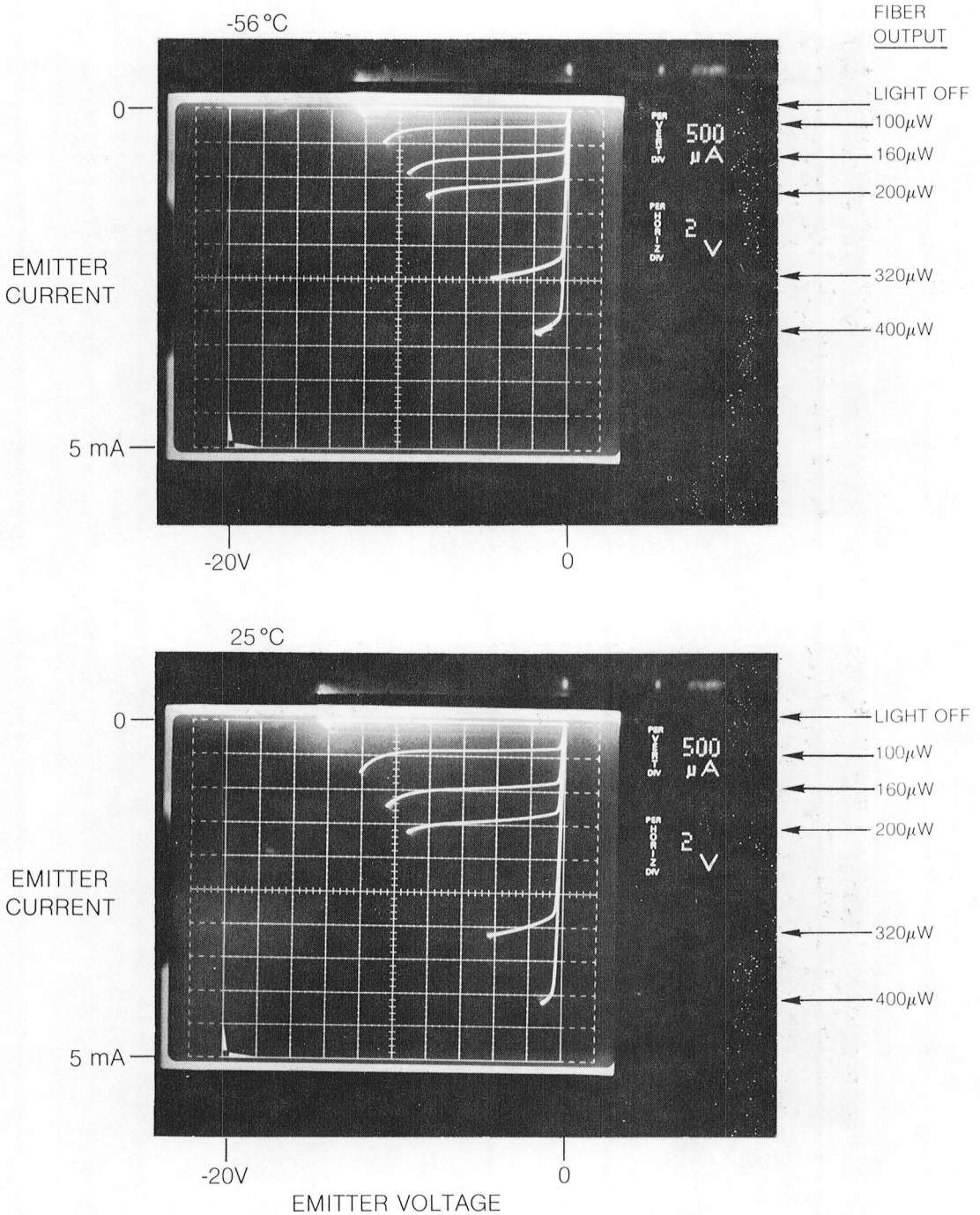
$\lambda = 8360\text{Å}$ (BREADBOARD IRED)



83-3-119-17

CURRENT-VOLTAGE CHARACTERISTICS FOR PHOTOTRANSISTOR K11d WITH f-o PIGTAIL

BASE FLOATING — COLLECTOR GROUNDED
$\lambda = 8360\text{Å}$ (BREADBOARD IRED)

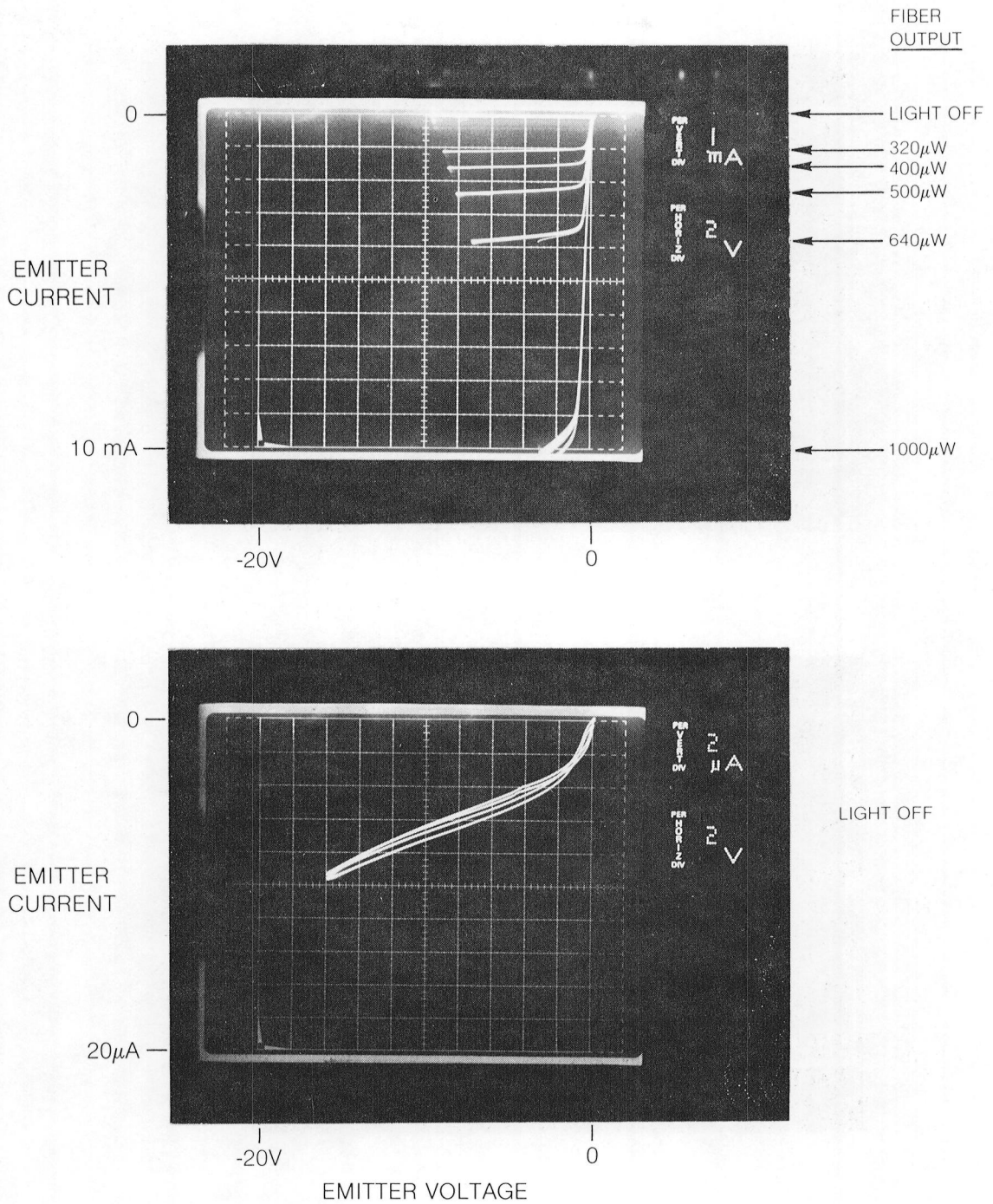


83-3-119-18

CURRENT-VOLTAGE CHARACTERISTICS AT 250°C FOR PHOTOTRANSISTOR R14a WITH f-o PIGTAIL

BASE FLOATING — COLLECTOR GROUNDED

$\lambda = 8360\text{Å}$ (BREADBOARD IRED)



83-3-119-19

FIG. 5-17

CURRENT-VOLTAGE CHARACTERISTICS FOR PHOTOTRANSISTOR R14a WITH f-o PIGTAIL

BASE FLOATING — COLLECTOR GROUNDED
λ = 8360Å (BREADBOARD IRED)

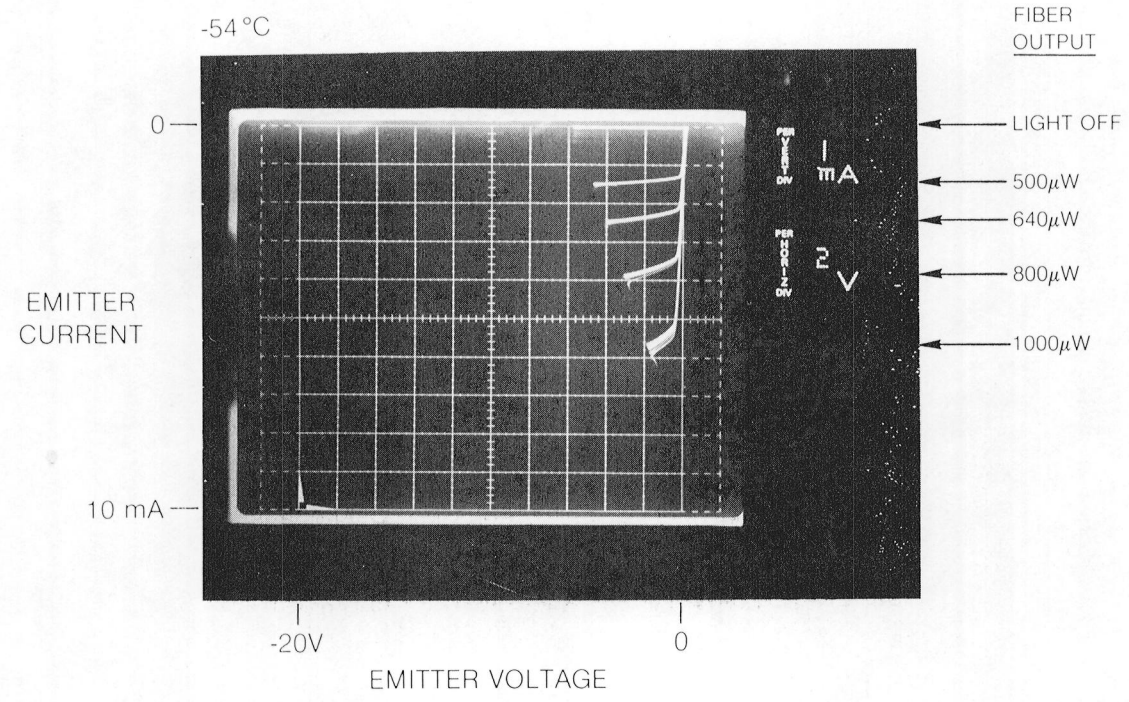
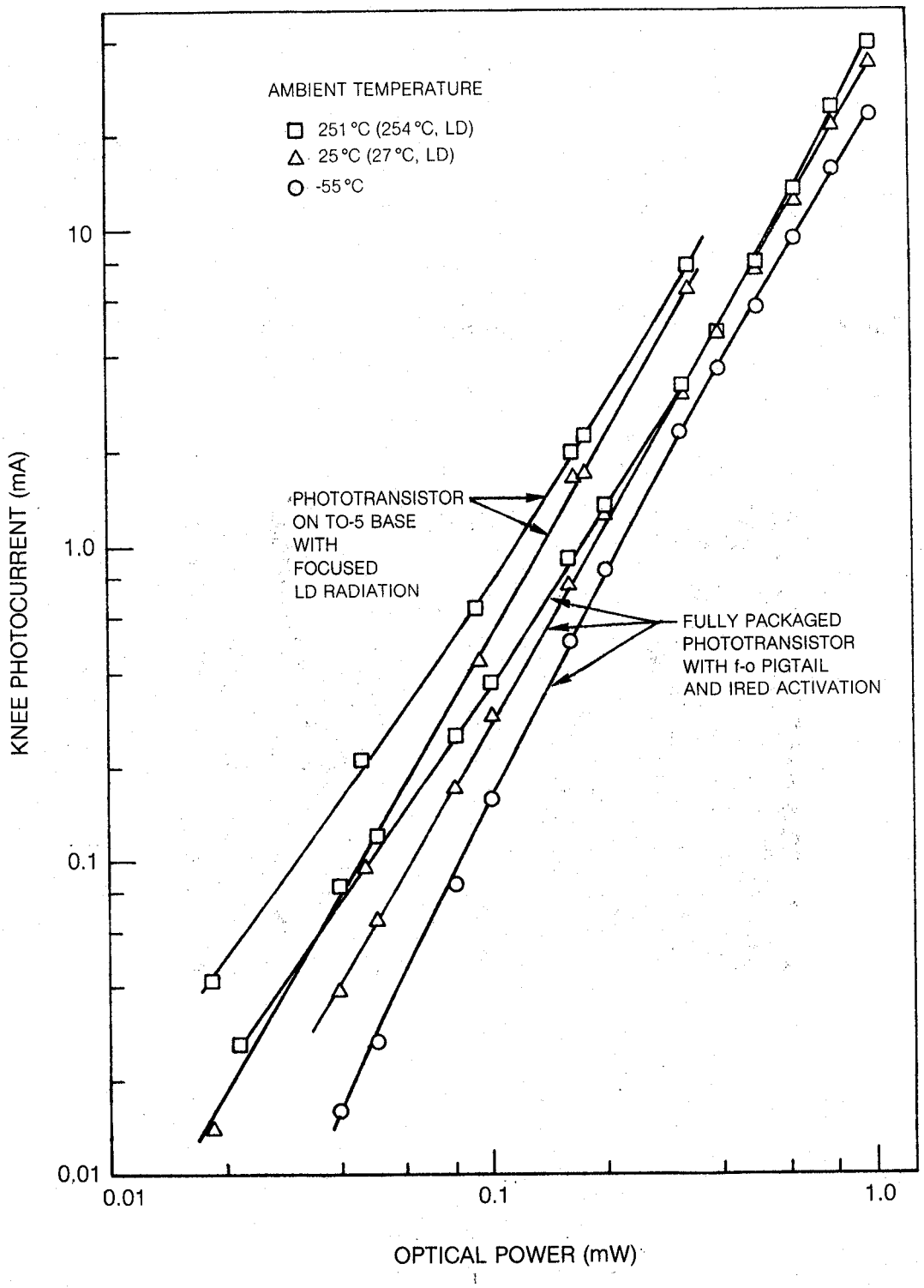


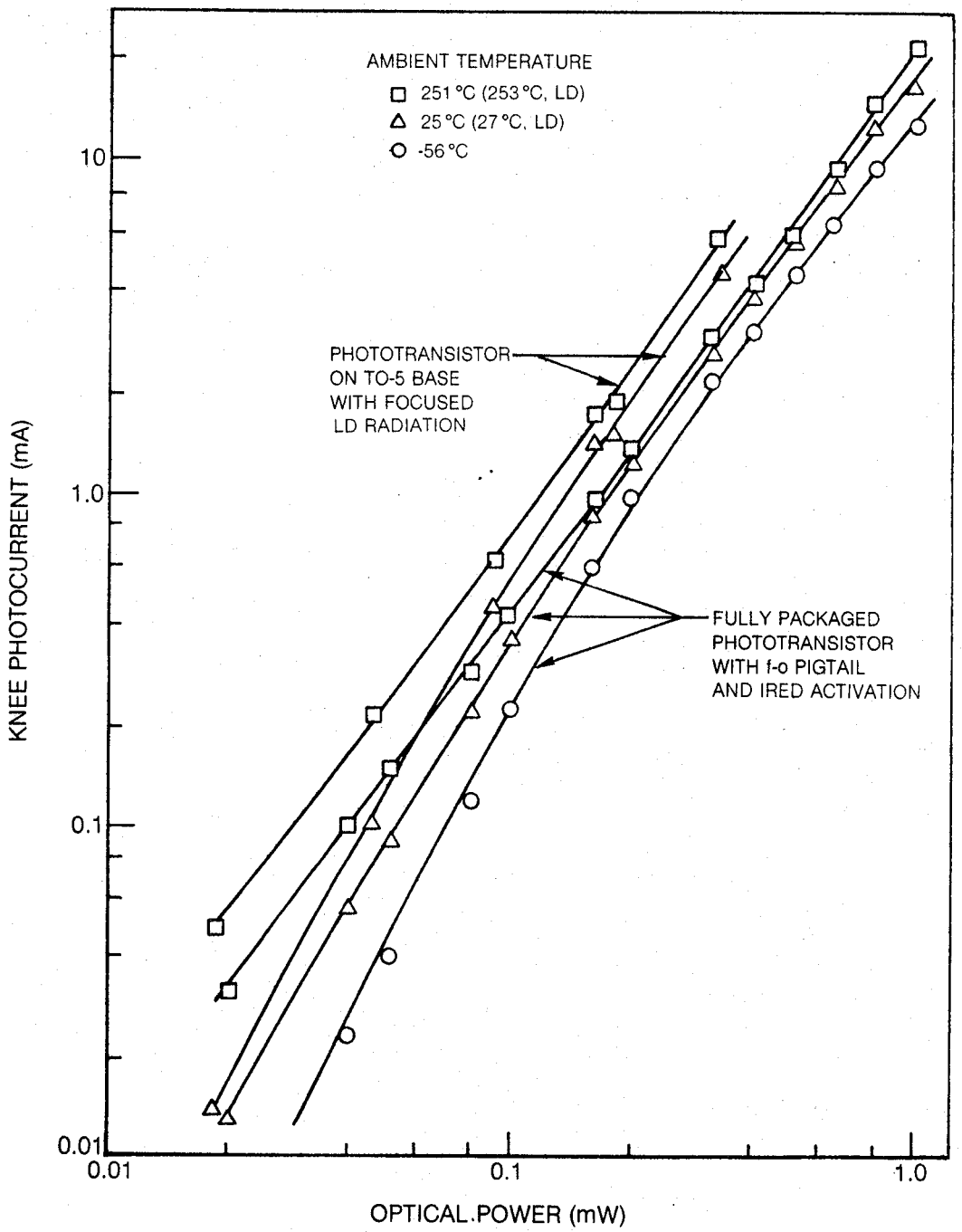
FIG. 5-18

PHOTOTRANSISTOR PHOTOCURRENT MEASUREMENTS (O13a)



82-8-34-1

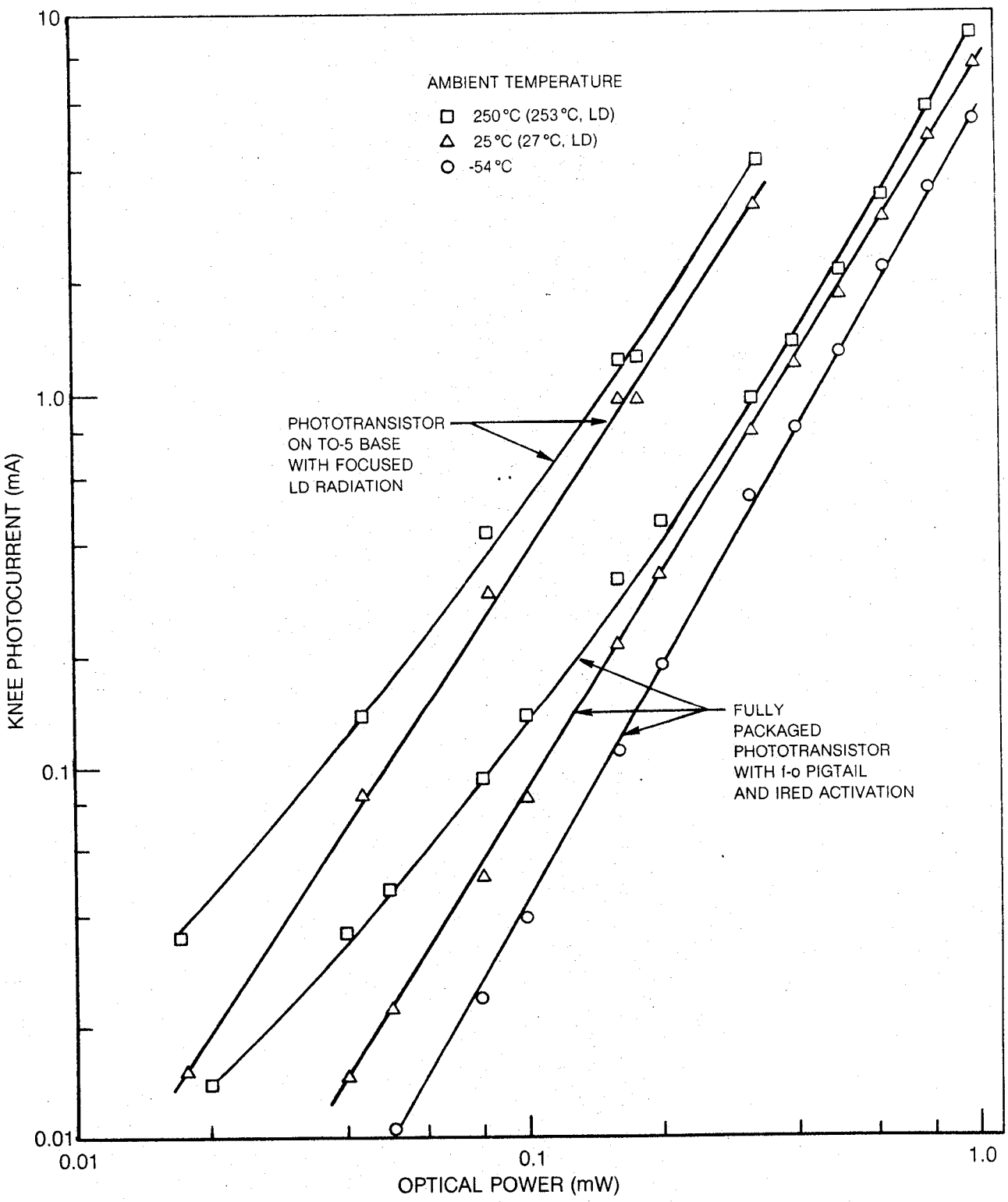
PHOTOTRANSISTOR PHOTOCURRENT MEASUREMENTS (K11d)



82-7-35-1

FIG. 5-20

PHOTOTRANSISTOR PHOTOCURRENT MEASUREMENTS (R14a)



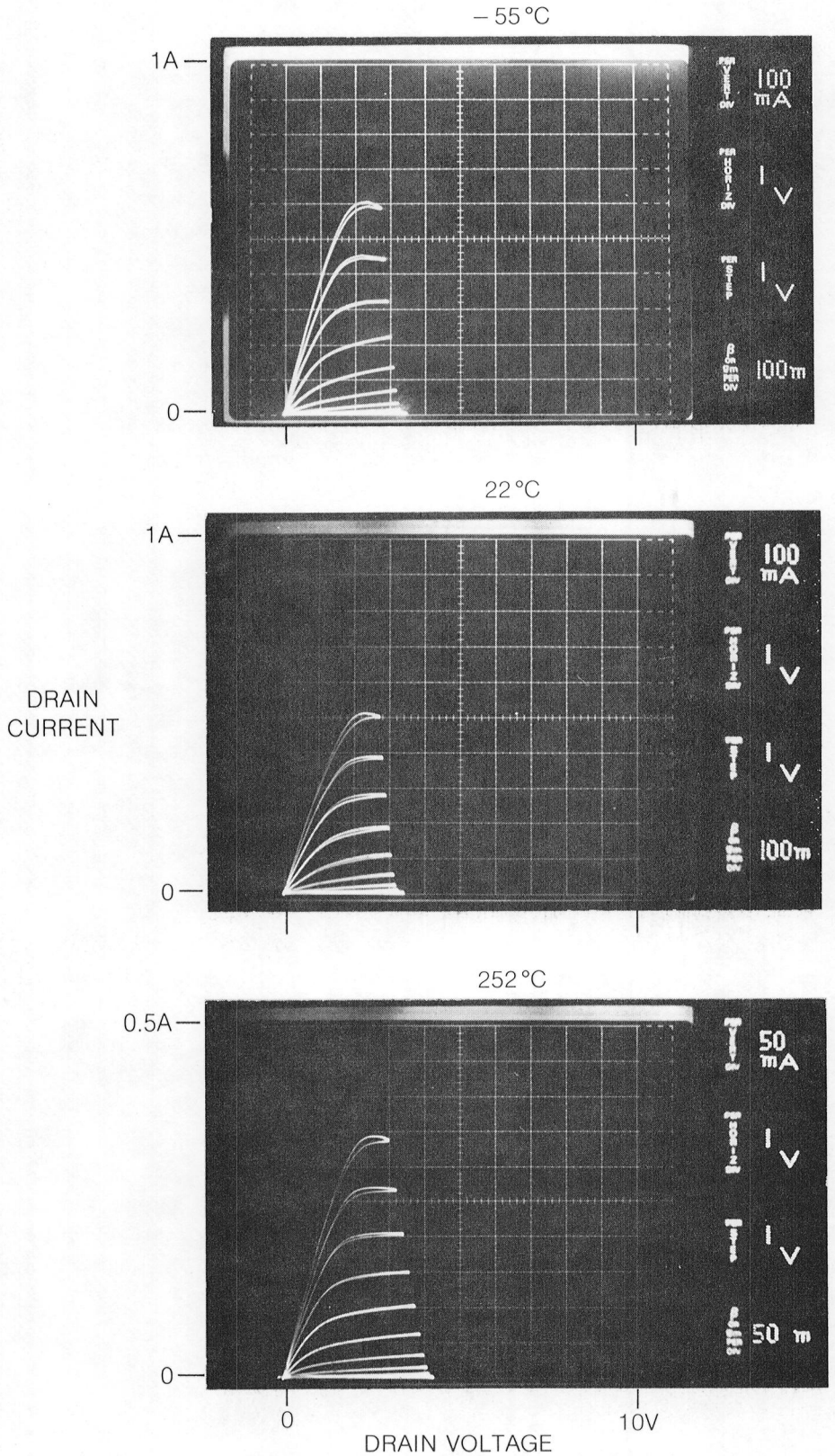
82-6-43-1

5.2 JFET Test Results

The breadboard demonstrator required GaAs JFET devices that could switch 100 mA into the torque-motor load and stand-off 20V on the device drain. JFET device goals were that gate voltage should be between -10V and -14V and that the on-state dc JFET resistance should be less than 10 ohms at 250°C. JFETs were selected principally for low off-state gate and drain leakage currents at 250°C. This established device integrity and led to higher circuit values for R_S (Fig. 3-3) and therefore lower required phototransistor output and IRED optical power. Packaged devices were first electrically screened at 250°C and at room temperature. The best devices were further tested at 250°C by an extended period of switching 100 mA of current with a +20V off-state drain voltage. This "burn-in" period was required to stabilize device leakage currents. The JFETs selected for this program were individually operated for more than 18 hours at 250°C at ~1700 Hz (50% duty cycle). Curve-tracer measurements of current-voltage characteristics were made during the testing periods to yield device current saturation, resistance, and gate and source-drain off-state leakage currents. After the room temperature and 250°C qualifications, the best devices were tested near -54°C and 175°C. Three devices were selected for delivery. These turned out to be the smallest device on each of the packaged GaAs chips. Each had a gate width of about 0.4 cm.

Current-voltage characteristics after the "burn-in" period for the delivered GaAs JFET devices are shown in Figs. 5-21 through 5-28. The first figure shows saturation currents for one device as a function of applied gate voltage. The upper curve in each figure is the zero-gate-bias result and each succeeding curve differs by -1V on the gate. (Eventually this device was shut off with a -14V gate voltage.) Saturation currents in both GaAs and silicon JFET devices decrease with increasing temperature; therefore, the device switching current must be compared to the on-state saturation current at 250°C. The maximum on-state JFET gate voltage in the Case-II circuit configuration is about -0.4 to -0.5V or in between the upper two curves of the saturation characteristics. The saturation current for JFET D7s at 252°C is estimated to be 300 mA which is sufficiently greater than the program requirement to assure device operation in the linear region of the curve. The current-voltage characteristics in the linear region are better shown in Fig. 5-22. At 100 mA the dc on-state JFET resistance, with correction for test-lead resistance, is estimated to be 1.9 ohms at -55°C and 4.6 ohms at 252°C. These device resistances were small compared to expected torque-motor coil resistances. During the on-state this JFET therefore dissipated 19 mW and 46 mW respectively at the tested temperatures. Figure 5-23 shows characteristics out to 20V. JFET steady-state power dissipation peaks at an intermediate gate voltage. During operation, the JFET is rapidly switched through the intermediate gate voltages so that the device power dissipation is largely

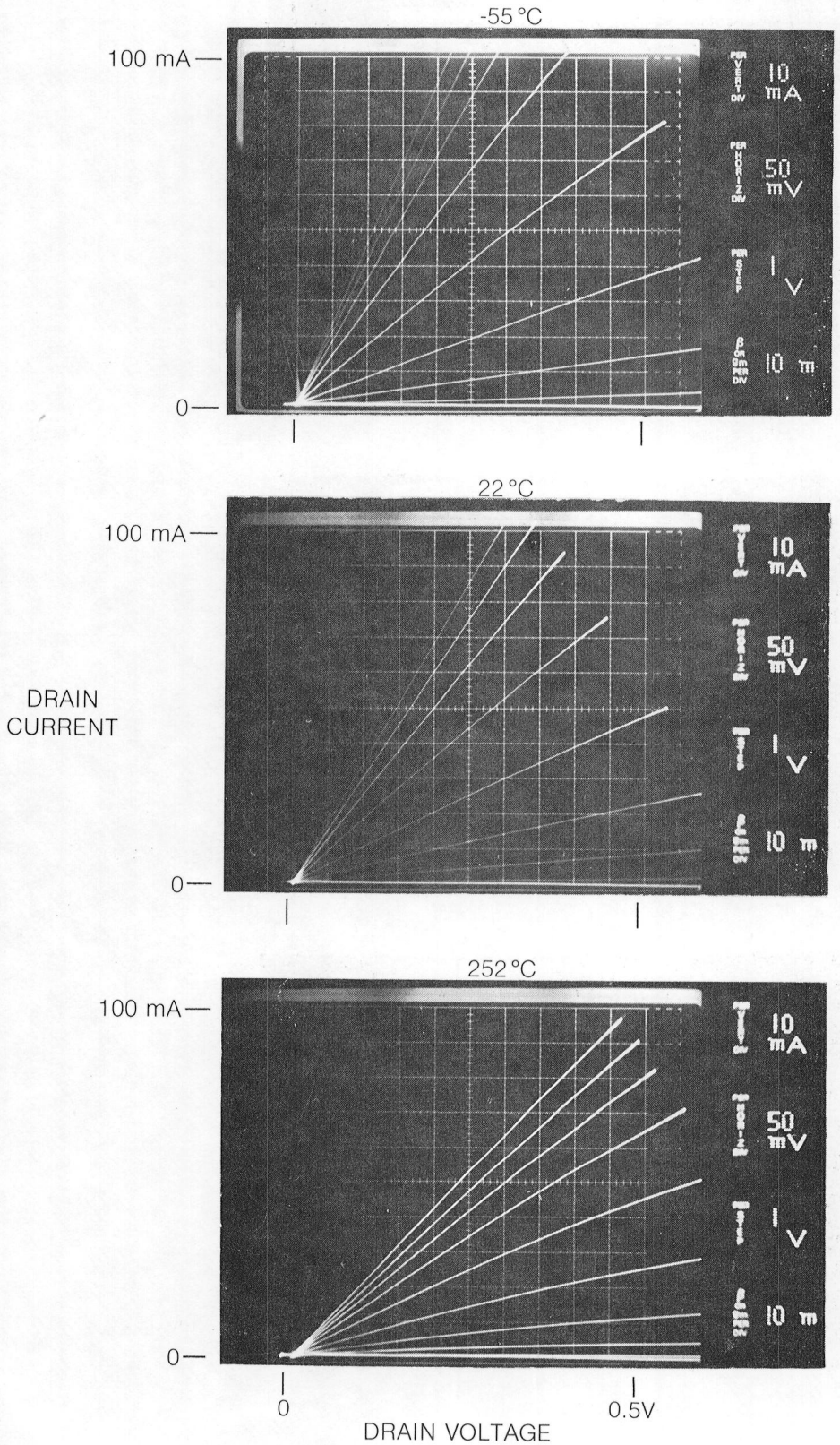
DRAIN SATURATION CHARACTERISTICS FOR GaAs JFET D7s



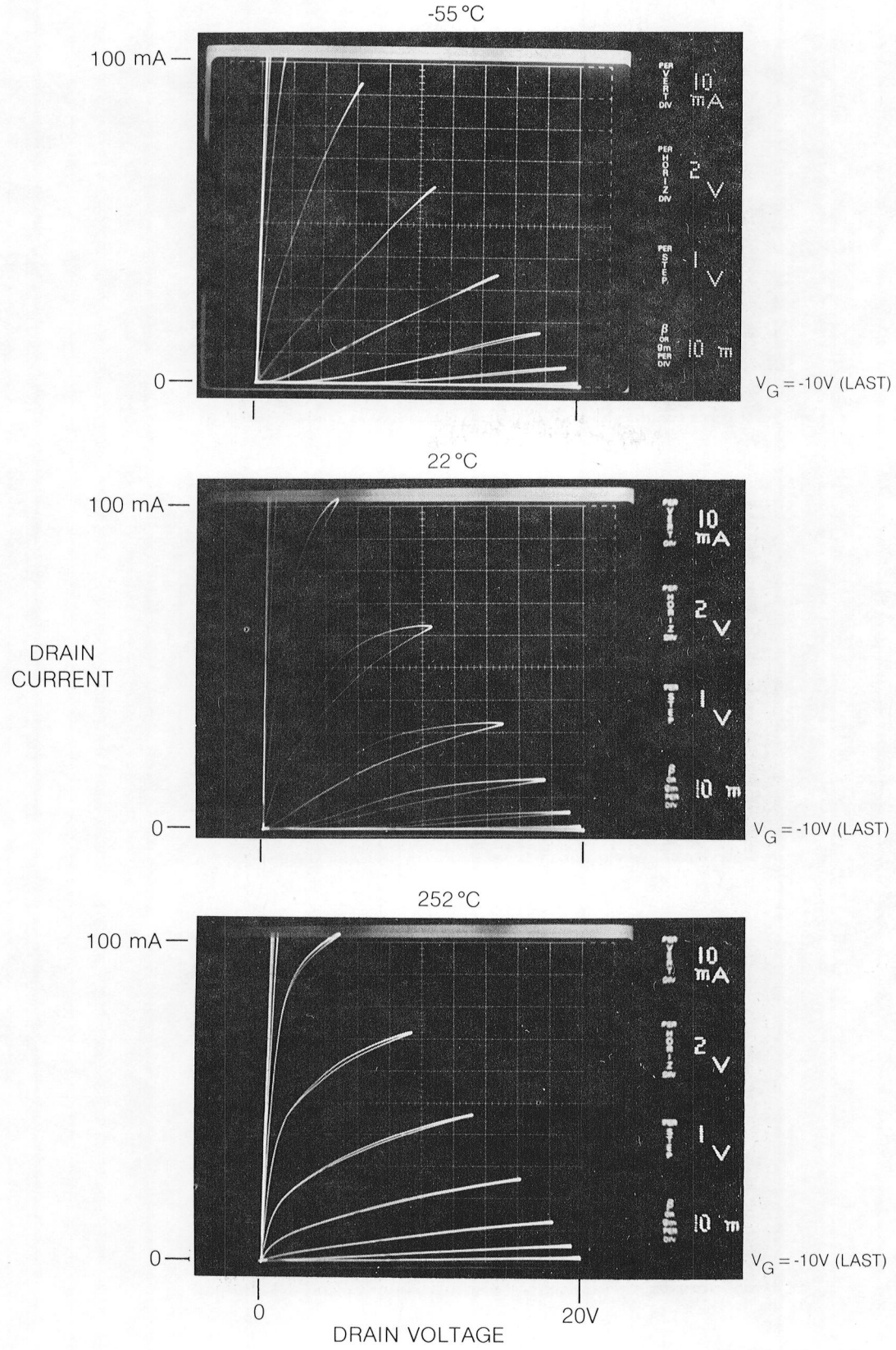
83–3–119–21

FIG. 5-22

CURRENT-VOLTAGE CHARACTERISTICS FOR GaAs JFET D7s

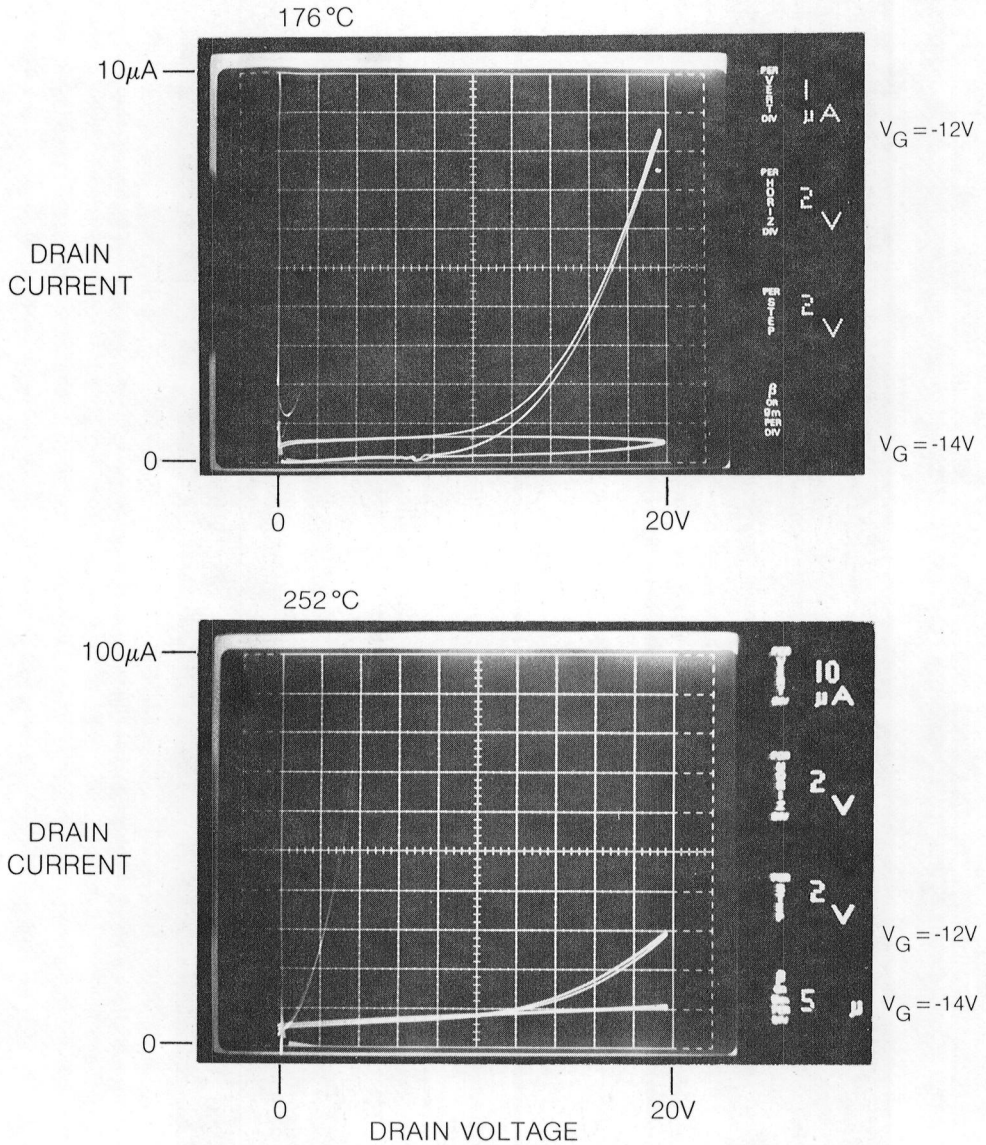


DRAIN CHARACTERISTICS FOR GaAs JFET D7s



83–3–119–23

LOW-LEVEL GaAs JFET CHARACTERISTICS (D7s)



83-3-119-24

DRAIN SATURATION CHARACTERISTICS FOR GaAs JFET

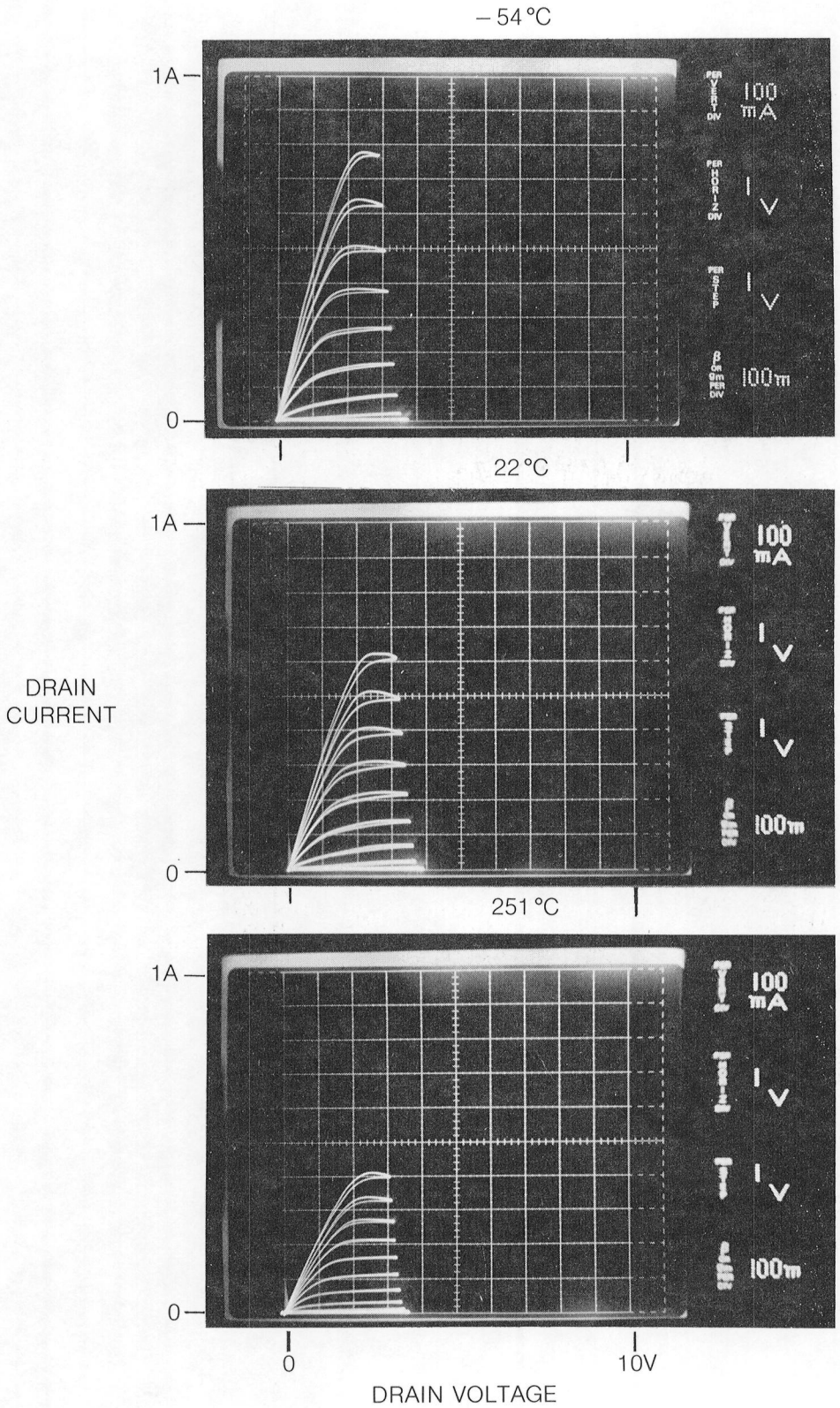
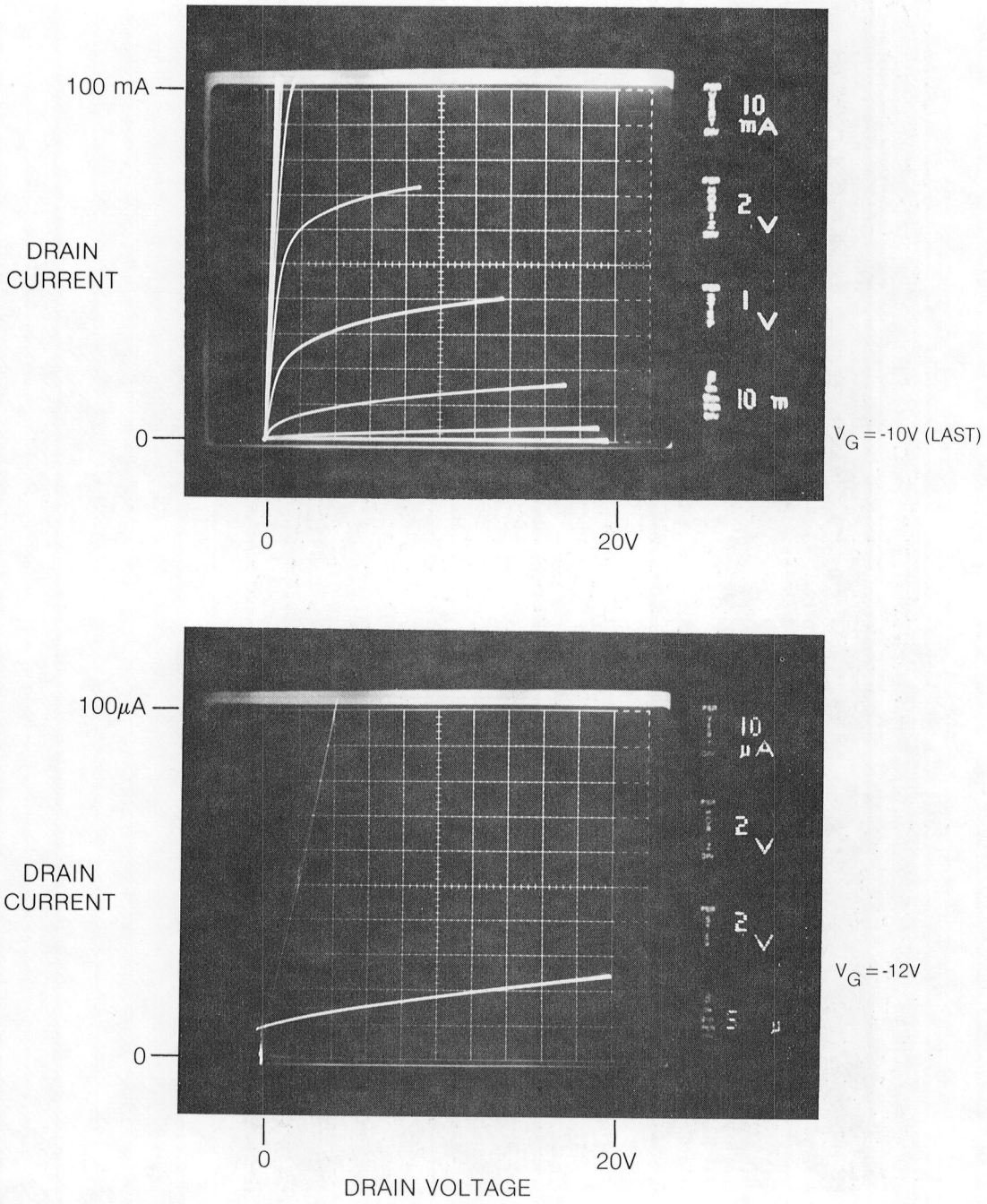
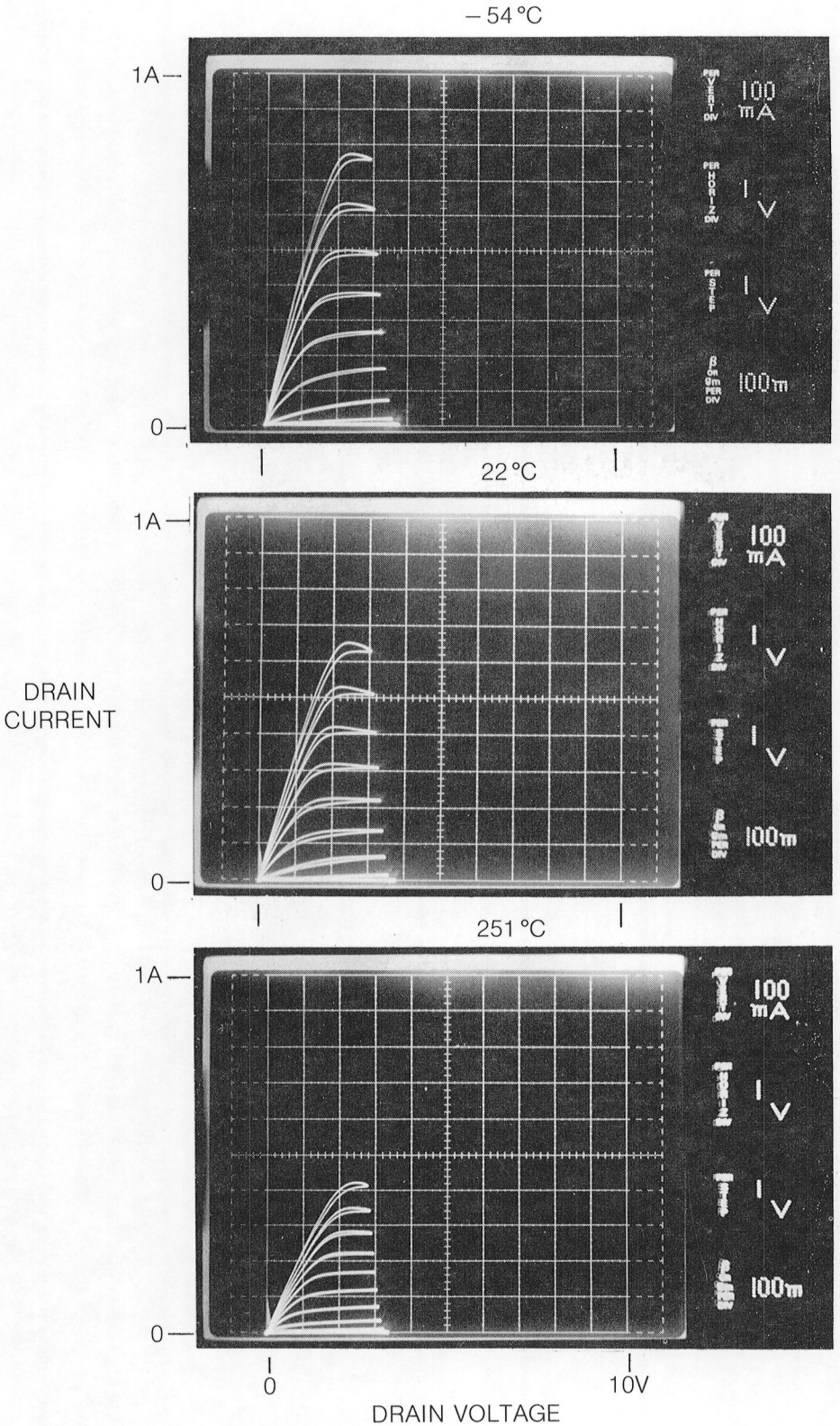


FIG. 5-26

DRAIN CHARACTERISTICS FOR GaAs JFET M8s AT 251°C



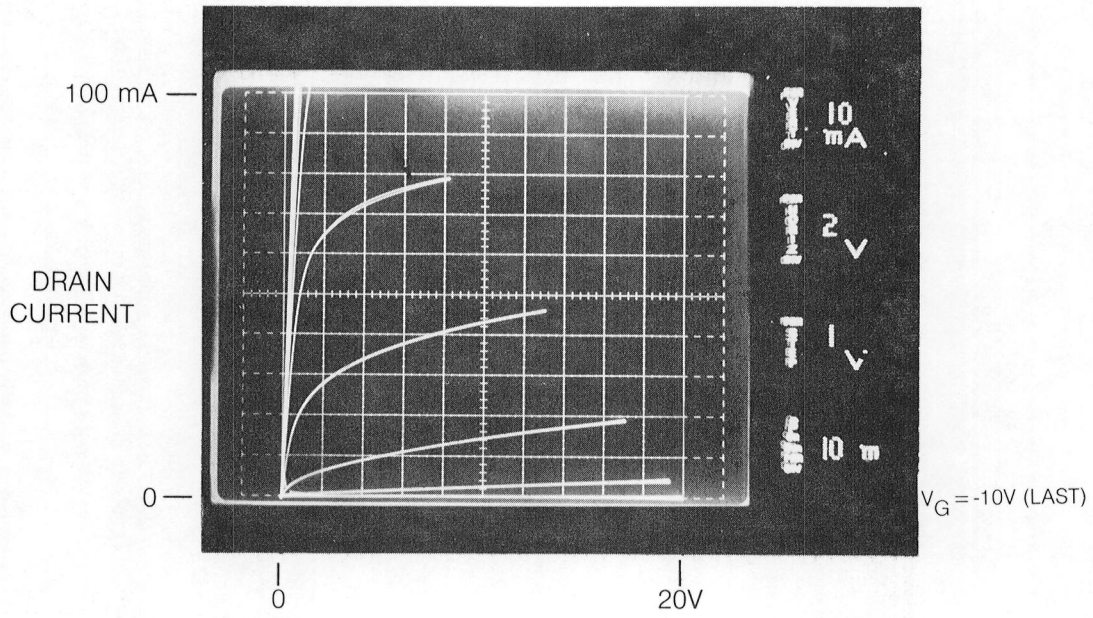
DRAIN SATURATION CHARACTERISTICS FOR GaAs JFET H6s

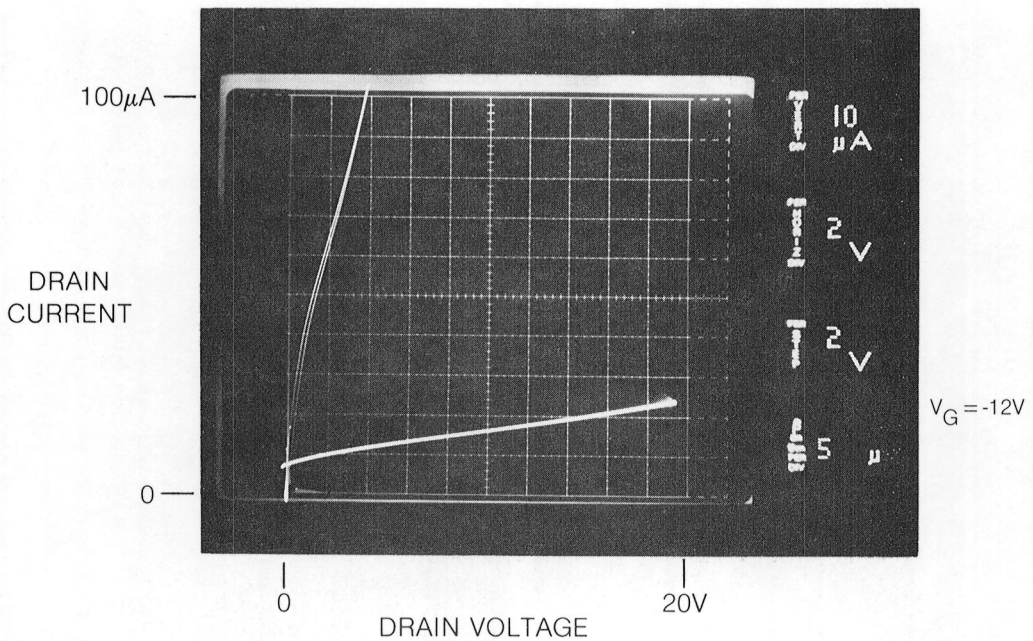


83–3–119–27

FIG. 5-28

DRAIN CHARACTERISTICS FOR GaAs H6s AT 251°C





83–3–119–28

due to the on-state -0.5V gate condition. The lower-level characteristics are shown in Fig. 5-24. The off-state source-drain current for this device with 20V on the drain was 10 μA. More common values for good devices were 20 μA to 70 μA. These values are small compared to the on-state current capability of 100 mA. The remaining figures up through Fig. 5-28 show the more important device characteristics of the other two delivered GaAs JFETs.

Tabular summaries of the important electrical properties measured after the "burn-in" period are shown in Tables IX and X. Table IX shows pinch-off voltage, current saturation, and dc resistance at four temperatures. The gate pinch-off voltage is the voltage that must be applied to turn-off or minimize (at high temperature) device source-drain current out to +20V on the drain. Generally, a slightly higher pinch-off voltage was observed as temperature increased. Part of this could have been due to changes in the exposed GaAs surfaces; however, part of this was experimental, in that the curve-tracer sensitivity during lower-temperature measurements was not high enough compared to actual off-state currents. Thus, the last traces of source-drain current could not be visually eliminated and the device appeared fully off at a lower gate voltage. The saturation currents, I_{Dsat}, are listed next. These are interpolated results for the on-state -0.5V gate condition. The dc resistances at the same gate condition and at 100-mA current flow are also shown. Device resistances increased only about a factor of 2.1 over the -55°C to 251°C temperature range. At the same time device saturation currents fell by about a factor of 1.8.

The high-temperature off-state GaAs JFET leakage currents with +20V on the drain near 178°C and 251°C are shown in Table X. The gate leakage was measured differentially across a resistor placed in series with the gate using an oscilloscope; the source-drain currents were obtained directly from the curve tracer. Measurements were taken near the pinch-off voltage using either a steady dc voltage on the gate or the stepped voltage from the curve-tracer base generator. Before the "burn-in" period, the off-state currents were higher. The leakage currents with the steady gate voltage showed the largest changes during the "burn-in" testing. These beneficial decreases appeared to be permanent.

A comparison of listings from Tables IX and X and Figs. 5-25 to 5-28 shows that JFETs, M8s and H6s had almost identical electrical characteristics. Device D7s had lower values for current saturation and device conductance but exhibited the lowest off-state leakage currents of all devices tested during this program.

TABLE IX

ELECTRICAL PARAMETERS FOR GaAs JFETs

	M8s	H6s	D7s
T (^{o}C)	Gate Pinch-Off Voltage (Volts)		
-55	-11.0	-12.0	-12.5
22	-11.6	-11.5	-13.0
177-9	-12.4	-12.3	-13.3
251-2	-12.4	-12.8	-13.1
	I_{Dsat} (mA) at V_G = -0.5V		
-55	700	690	520
22	560	570	450
177-9	430	430	350
251-2	370	380	300
	DC Resistance (ohms) at V_G = -0.5V and I_D = 100 mA		
-55	1.9	1.9	2.1
22	2.4	2.3	2.8
177-9	3.4	3.2	3.9
251-2	3.9	3.8	4.6

TABLE X

OFF-STATE LEAKAGE CURRENTS FOR GaAs JFETs

Gate V	T(°C)	M8s		H6s		D7s	
		Gate Current at V_G (V_D = 20V)					
		μA	V_G(Volts)	μA	V_G(Volts)	μA	V_G(Volts)
Steady	177-9	2	-12.4	4	-12.3	1	-13.3
Steady	251-2	40	-12.4	50 42	-12.8 -12.0	10	-13.2
Stepped	177-9	2.5	-12.0	4	-12.0	1.5	-14.0
Stepped	251-2	52	-12.0	56	-12.0	13	-14.0
		Source-Drain Current at V_G (V_D = 20V)					
Steady	177-9	1.4	-12.4	1.3	-12.3	0.6	-13.3
Steady	251-2	24	-12.4	23 28	-12.8 -12.0	12	-13.2
Stepped	177-9	1.4	-12.0	1.1	-12.0	0.5	-14.0
Stepped	251-2	24	-12.0	24	-12.0	10	-14.0

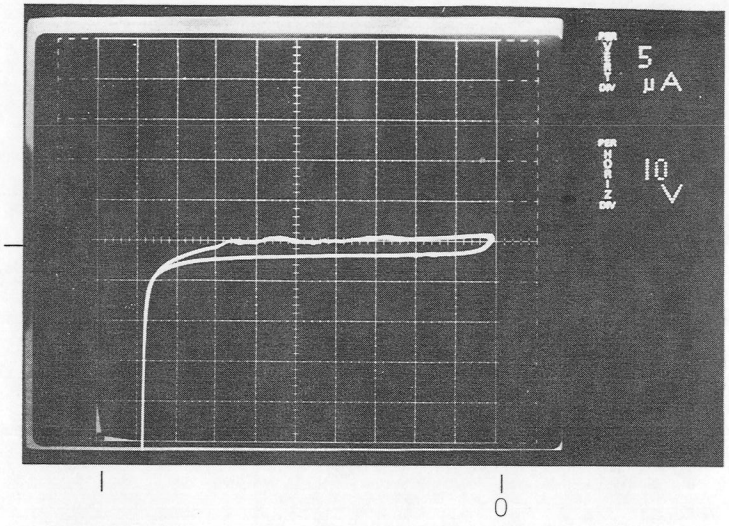
5.3 Testing of Transient-Protection Diodes

A GaAs transient-protection diode was required in the photoswitch system to prevent the GaAs JFET drain from rising to destructively high voltages during inductive load switching. The highest reverse-bias voltage across the diode during switching was 20V. For safety a 50V reverse-bias capability over the operating temperature range was established as a device goal. The highest possible forward current through the diode was 100 mA (JFET switching current) which would only be reached under infinitely fast switching. Device integrity was indicated by the magnitude of the leakage currents near 250°C and at high reverse bias. For a given diode size, electrial characteristics were very similar for devices selected for test from the source GaAs wafer; therefore, the value of high-temperature leakage current near breakdown was a principal factor in diode selection. The 115-μm-diameter mesa size was selected for breadboard application. Using Eq. 3-4 and coil inductance = 0.1H, coil current = 0.1A, ℓ_s = 350 μm, frequency = 100 Hz, and r_d = 57.5 μm, then a steady-state diode temperature increase of 50°C would result if all the inductive power were dissipated in the diode. In actual practice the power will be dissipated in the resistive portions of the circuit which include the load as well. Based on the diode forward characteristics and an anticipated load resistance (20V/0.1A) for the breadboard demonstrator, only a 3°C diode temperature increase above ambient was expected.

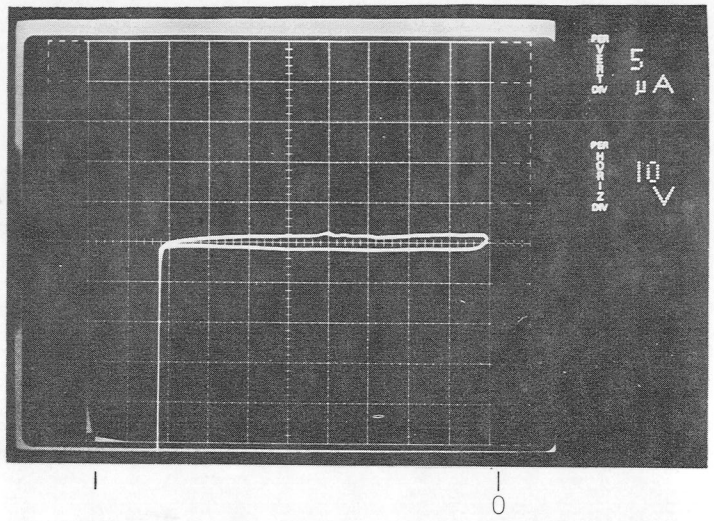
Packaged diodes were tested over the -55°C to 251°C range and were selected for delivery based on quality of the measured current-voltage characteristics. The characteristics for one of the diodes are given in Figs. 5-29 and 5-30. The reverse breakdown characteristics are sharp at -55°C and 23°C with a noticeable rounding occurring at 178°C and more at 251°C. The breakdown voltages at these temperatures are -57V, -67V, -82V, and -88V respectively, which are above the device goal of -50V. The increase in breakdown voltage with increasing temperature is characteristic of semiconductor diodes (Ref. 1, Chapter 2). At 251°C, the reverse current at -20V (the maximum switching voltage) was 0.8 μA. This value was taken from another I-V characteristic and is negligible compared with an inductive load current of 100 mA. Figure 5-30 shows the forward characteristics. Since the highest possible current through the diode is 100 mA, the maximum voltage that can be added to the JFET drain while dissipating inductive power is the diode voltage at 100 mA. This is seen to vary from 1.18V at 251°C to 1.93V at -55°C. This will add a small amount of JFET source-drain and gate leakage to the values of Table X, which were obtained at V_D = +20V. The other two deliverable transient-protection diodes showed similar current-voltage characteristics (Fig. 5-31). Table XI summarizes the testing results for the three deliverables. The electrical characteristics are very uniform. The noticeable difference was at 250°C in the rounding of the reverse-bias current-voltage curves at breakdown which led to more noticeable leakage current variations. Reverse leakage currents at 177°C were about 1 μA at $-V_B$ and were not accurately measurable at -20V.

REVERSE CURRENT-VOLTAGE CHARACTERISTICS FOR GaAs DIODE D1s

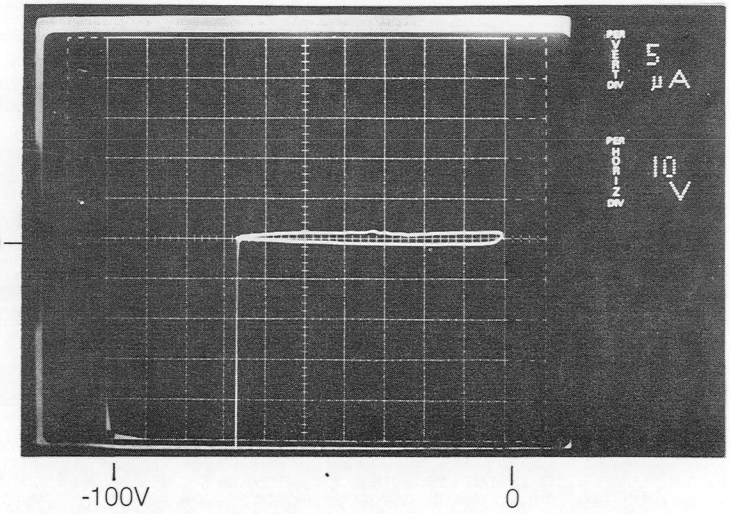
a) 251 °C



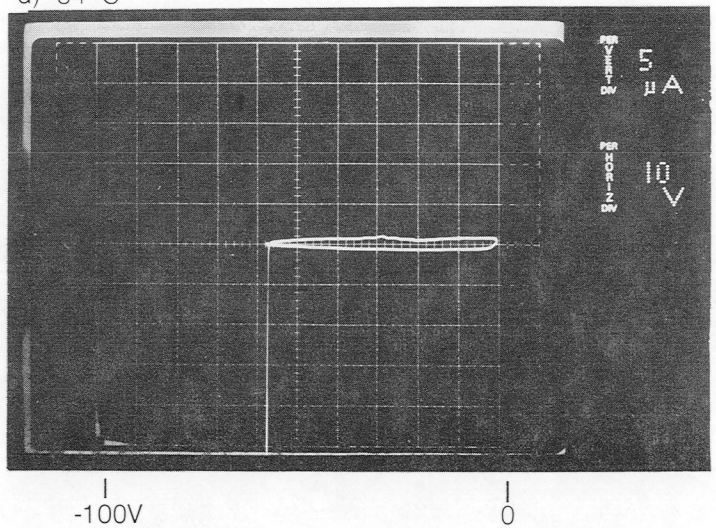
b) 178 °C



c) 23 °C



d) -54 °C

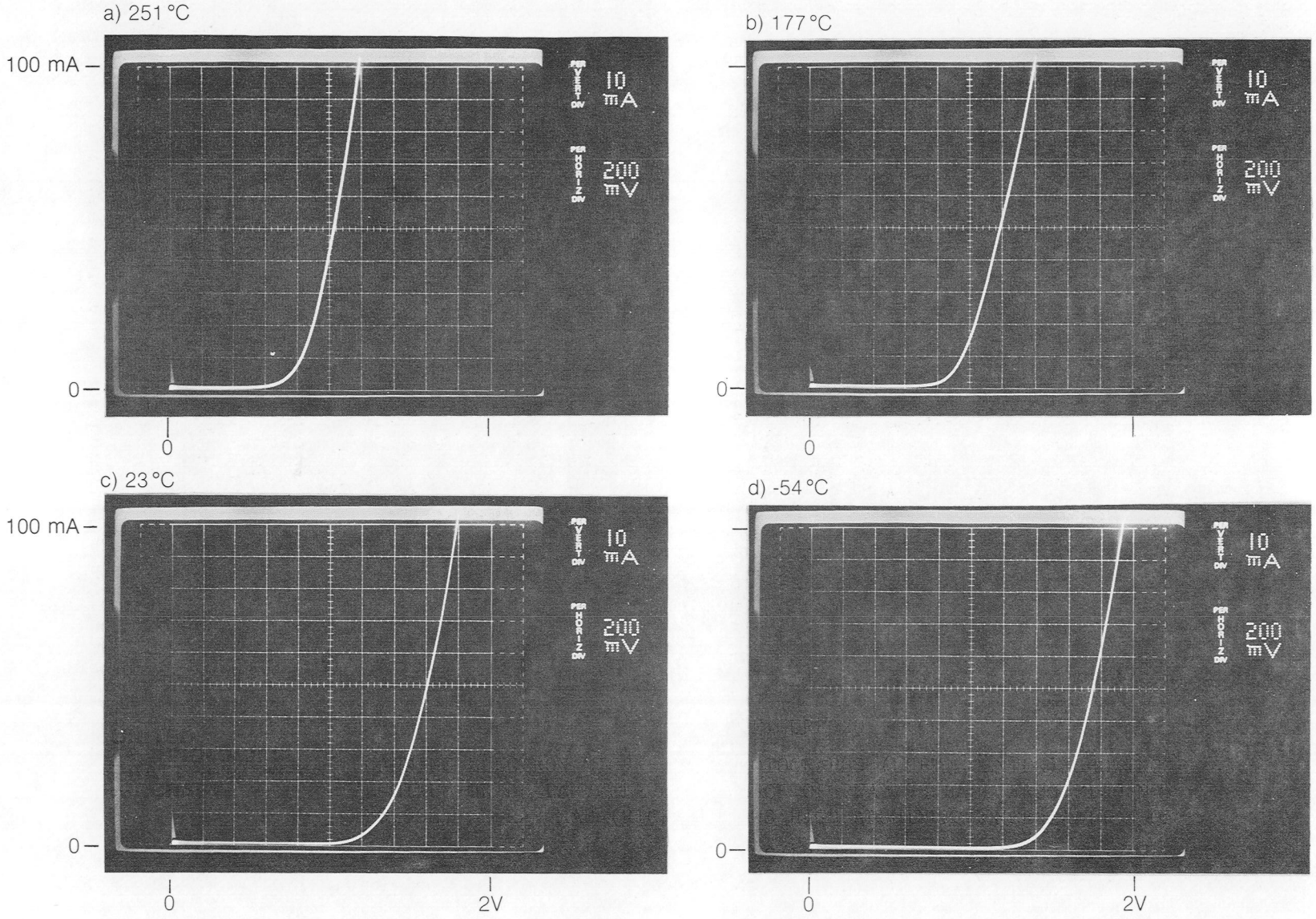


81-4-16-2

R83-925312-25

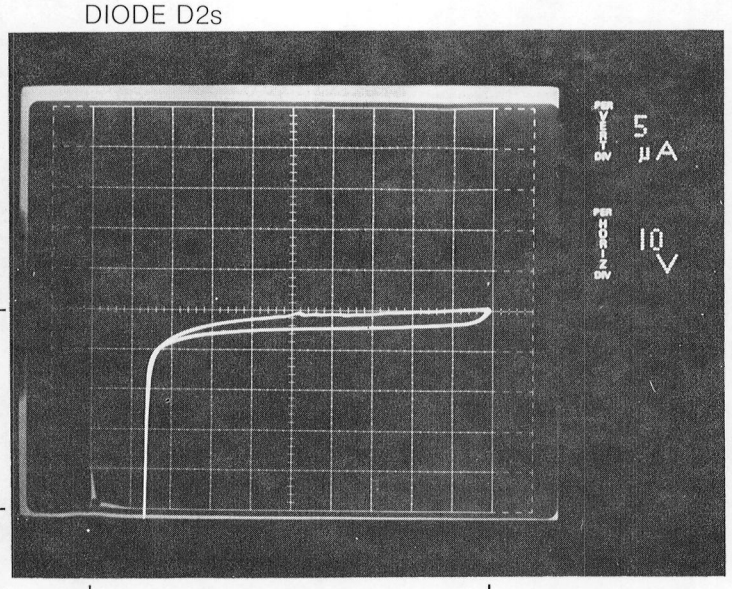
FIG. 5-29

FORWARD CURRENT-VOLTAGE CHARACTERISTICS FOR GaAs DIODE D1s

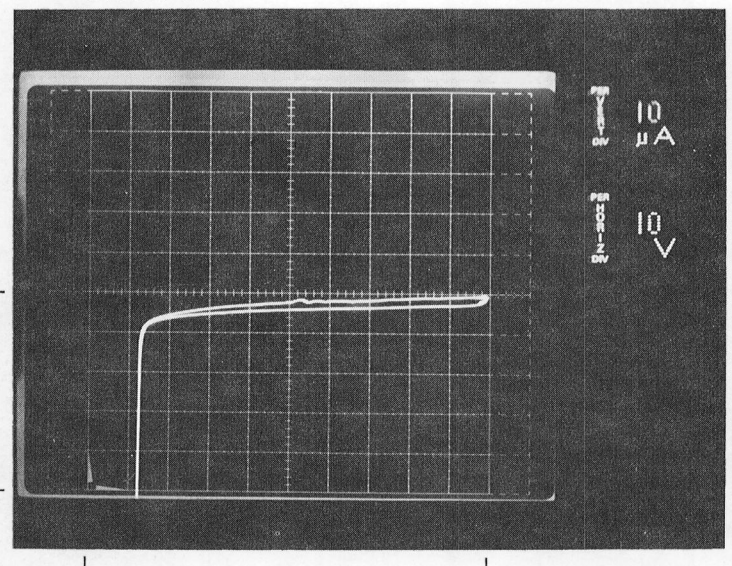


REVERSE DIODE CHARACTERISTICS AT 251°C

DIODE D2s



DIODE D3s



VOLTAGE

83-3-119-29

TABLE XI

ELECTRICAL PARAMETERS FOR GaAs DIODES

(115-μm diameter)

	D1s		D2s		D3s	
T(°C)	Reverse Breakdown Voltage (V_B, Volts)					
-54	-57		-55		-56	
23	-67		-64		-65	
178	-82		-80		-81	
251	-88		-86		-87	
	Reverse Leakage Current (μA)					
	-20V	V_B	-20V	V_B	-20V	V_B
178	--	~1	--	~1	--	~1
251	0.6	5	0.6	6	1	8
	Forward Voltage at I = 100 mA (Volts)					
-54	1.93		1.94		1.99	
23	1.78		1.80		1.85	
178	1.38		1.38		1.41	
251	1.18		1.20		1.20	

6.0 BREADBOARD TESTING OF PHOTOSWITCH SYSTEM AND DISCUSSION OF RESULTS

The purpose of breadboard testing was to demonstrate fiber optic switching of current into a torque-motor load using high-temperature-capability photoswitch devices fabricated during this program. The switching was to be compatible with pulse-width modulation techniques used in aircraft digital electronic control. Breadboard testing included verification of photoswitch operation between -54°C and 250°C and verification of photoswitch endurance, 2 hours of continuous running at an ambient temperature of 250°C.

A full description of the breadboard is given in Appendix A of this report. This apparatus consisted of a table-mounted testing rack to provide electrical and optical power, a high-temperature probe assembly tethered to the rack, and three sets of high-temperature GaAs photoswitch devices. Each device set consisted of a photosensitive element (GaAlAs/GaAs phototransistor), a power device (GaAs JFET) and a transient-protection diode (GaAs mesa diode). With a device set mounted on the probe assembly, digital pulsing of the phototransistor with infrared light from the breadboard IRED was used to switch current into the torque-motor load. Prior to breadboard testing, the photoswitch devices passed through a qualification process involving considerable testing in the required temperature range, especially at 250°C. These procedures and results were the subject of Chapter 5.0. Of particular importance for breadboard testing were the pinch-off voltage of the JFET's, calibration curves of photogenerated knee photocurrents versus optical power for each of the packaged phototransistors (Figs. 5-18 to 5-20), and breadboard IRED calibration curve (Fig. A-2). The relevant information is listed in Table XII. About 1.3 mA of photogenerated phototransistor current was required on the breadboard. This corresponded to 240 μW to 510 μW of optical power emitted from the fiber inside the phototransistor packages. The recommended breadboard IRED current level was 50% higher than the minimum calibration IRED current at -54°C. Breadboard operation required that the following levels were set: (1) the IRED current to give the proper optical output for the particular phototransistor, (2) the gate voltage for the particular JFET, and (3) JFET drain current (and voltage) to give rated current through the torque-motor coils.

The GaAs photoswitch devices were connected as shown in Fig. A-4. The closest match to the 100-mA switching current goal was obtained by parallel arrangement of a set of torque-motor coils, which were rated at 80-mA total current. In order to demonstrate the system's higher-voltage capability, a resistor was added in series with the torque-motor coils. The resultant load required 18 to 19V drain voltage to obtain the 80-mA of switched current. The GaAs JFET's had been qualified for 100-mA operation and +20V stand-off voltage. The breadboard enabled monitoring of important circuit parameters at

TABLE XII

PHOTOSWITCH OPERATING PARAMETERS

A. Off-state pinch-off voltage (V_p) for GaAs JFET's between -54°C and 250°C.

JFET Device	V_p
D7s	-13.0
M8s	-12.0
H6s	-12.5

B. Calibration values (NOT BREADBOARD OPERATING VALUES) for phototransistors at each temperature (obtained from Figs. 5-18 to 5-20 and Fig. A-2).

	Minimum Levels for 1.3 mA Photocurrent					
	Optical Power (μW)			IRED Current (mA)		
Phototransistor	250°C	25°C	-54°C	250°C	25°C	-54°C
013a	200	210	240	22	23	26
K11d	200	210	250	22	23	27
R14a	380	410	510	42	46	59

C. Recommended Breadboard IRED Current

Phototransistor	IRED Current (mA)
013a	40
K11d	40
R14a	90

all times during photoswitching. These included JFET gate voltage, IRED current, JFET drain (coil) current, JFET drain voltage, phototransistor emitter voltage, and JFET gate current.

The pulse generator used to drive the breadboard IRED was capable of a repetition rate of 0.1 to 20 MHz with a continuously variable pulse width between 25 ns and 100 ms. Under actual dynamic operation in control systems the pulse width could vary with time. The test simulation using the pulse generator allowed constant pulse widths for a given generator setting; however, pulse width could be redefined by manually readjusting the generator. The pulse generator was equipped with a pulse-burst mode of operation which provided a preselected number of pulses after the receipt of a trigger. This feature was used to simulate static operation where steady-state conditions are maintained using a burst of pulses from the control computer. The pulse frequency could also be varied to allow operation at any frequency above and below the break frequency of the torque-motor coils. The rise time of the pulser and speed of all the GaAs devices were orders of magnitude faster than the maximum anticipated frequency of about 2 kHz for torque-motor switching in engine control applications. The actual test frequency at which most of the breadboard data were obtained was 40 Hertz at 50% duty cycle (pulse width of 12.5 msec).

For breadboard testing, each set of GaAs photoswitch devices was mounted on the probe assembly and placed in an oven at 250°C. When thermally equilibrated the devices were tested for a 2-hour minimum period at 250°C. The assembly was then cooled to room temperature and photoswitching was terminated. After preparation of a low-temperature bath, the photoswitch assembly was cooled to -54°C and photoswitching and data acquisition were resumed. After about 15 minutes of operation the photoswitch probe was removed to room temperature and testing was terminated. Item 2 of Table XIII summarizes the GaAs device content of each set as well as actual breadboard test values for V_p, IRED current and estimated optical power inside each phototransistor package.

During the period of temperature stabilization, device switching data were accumulated using an oscilloscope. Occasionally the pulse frequency and duty cycle were changed or pulse-burst operation initiated. Figure 6-1 illustrates switching action using GaAs device Set B at 253°C. The photographs illustrating breadboard switching at the other test temperatures look identical to those in Fig. 6-1. Except for the magnitudes of the gate pinch-off voltage and required IRED current, the two other GaAs photoswitch sets also showed identical breadboard switching characteristics. When the phototransistor was illuminated, there was a near-zero voltage on the JFET gate and current flowed through the torque motor. Negative voltage (V_p) on the gate (illumination off) terminated current flow through the torque motor.

TABLE XIII

PHOTOSWITCH BREADBOARD TEST DATA

1. Electrical Test Conditions

40 Hertz, 50% Duty Cycle
80 mA into Torque-Motor Load
18-19V off-state JFET drain voltage

2. GaAs Device Sets and Additional Operational Conditions

Set	Phototransistor	JFET	Diode	V_p (V)	Current (mA)	Optical Power (μW)*
A	R14a	D7s	D1s	-13.2 to -13.5	95	760
B	013a	M8s	D3s	-12.0 to -12.5	38	350
C	K11d	H6s	D2s	-12.5 to -12.8	38	350

3. Temperature Data

Set	Temp (°C)	ΔV_D (V)	$V_{G,on}$ (V)	$I_{G,off}$ (μA)
A	250	0.7	-0.24	27
	25	1.0	-0.16	**
	-55	1.2	-0.15	**
B	253	0.7	-0.23	37
	24	1.0	-0.15	**
	-55	1.3	-0.12	**
C	252	0.7	-0.24	42
	23	1.1	----	**
	-54	1.3	-0.14	**

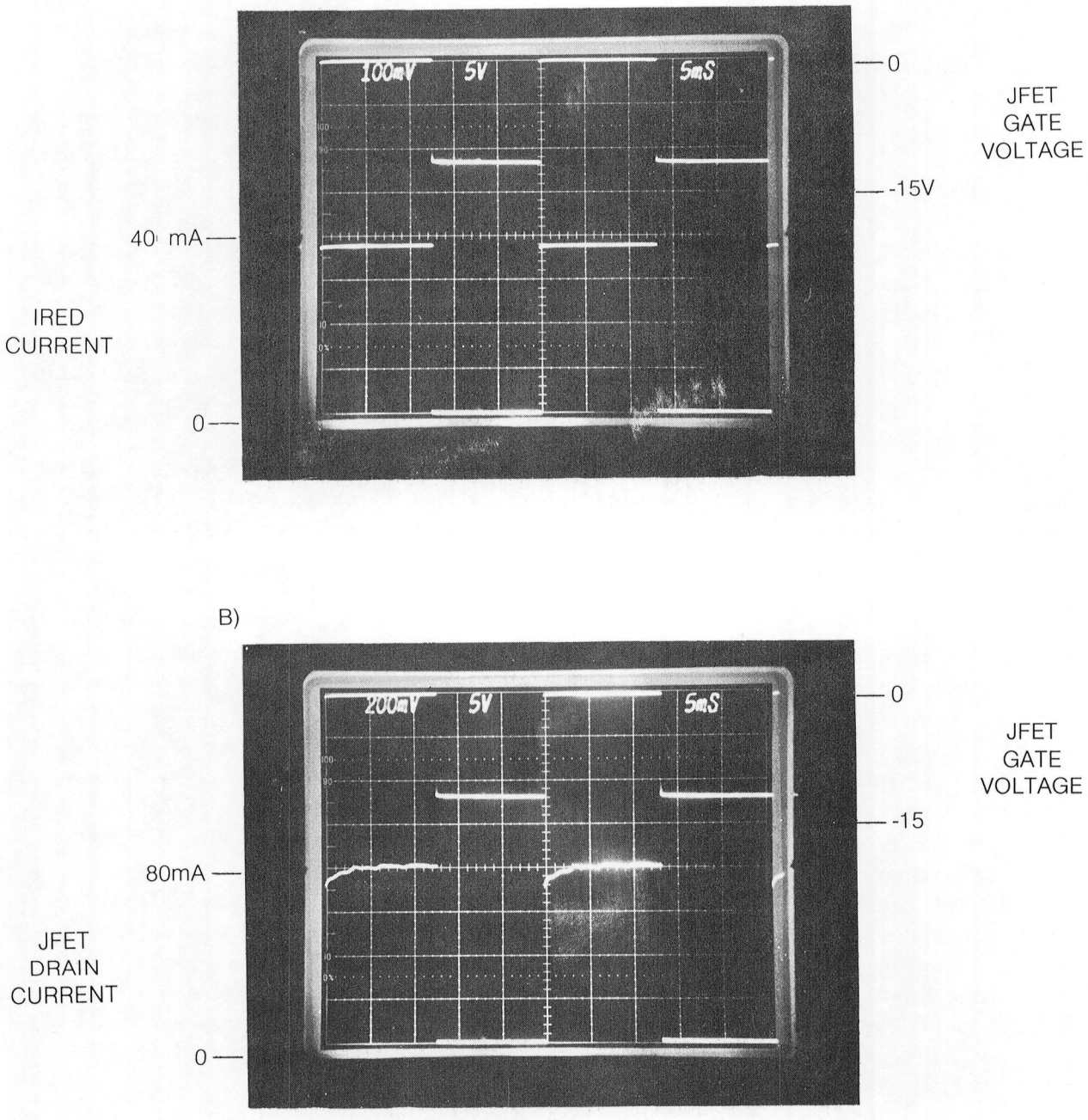
* estimated emission from optical fiber inside sealed phototransistor package

** Less than 1 μA (measurement sensitivity)

FIG. 6-1

BREADBOARD PHOTOACTIVATED SWITCHING

GaAs DEVICE SET B AT 253 °C



82-10-9-2

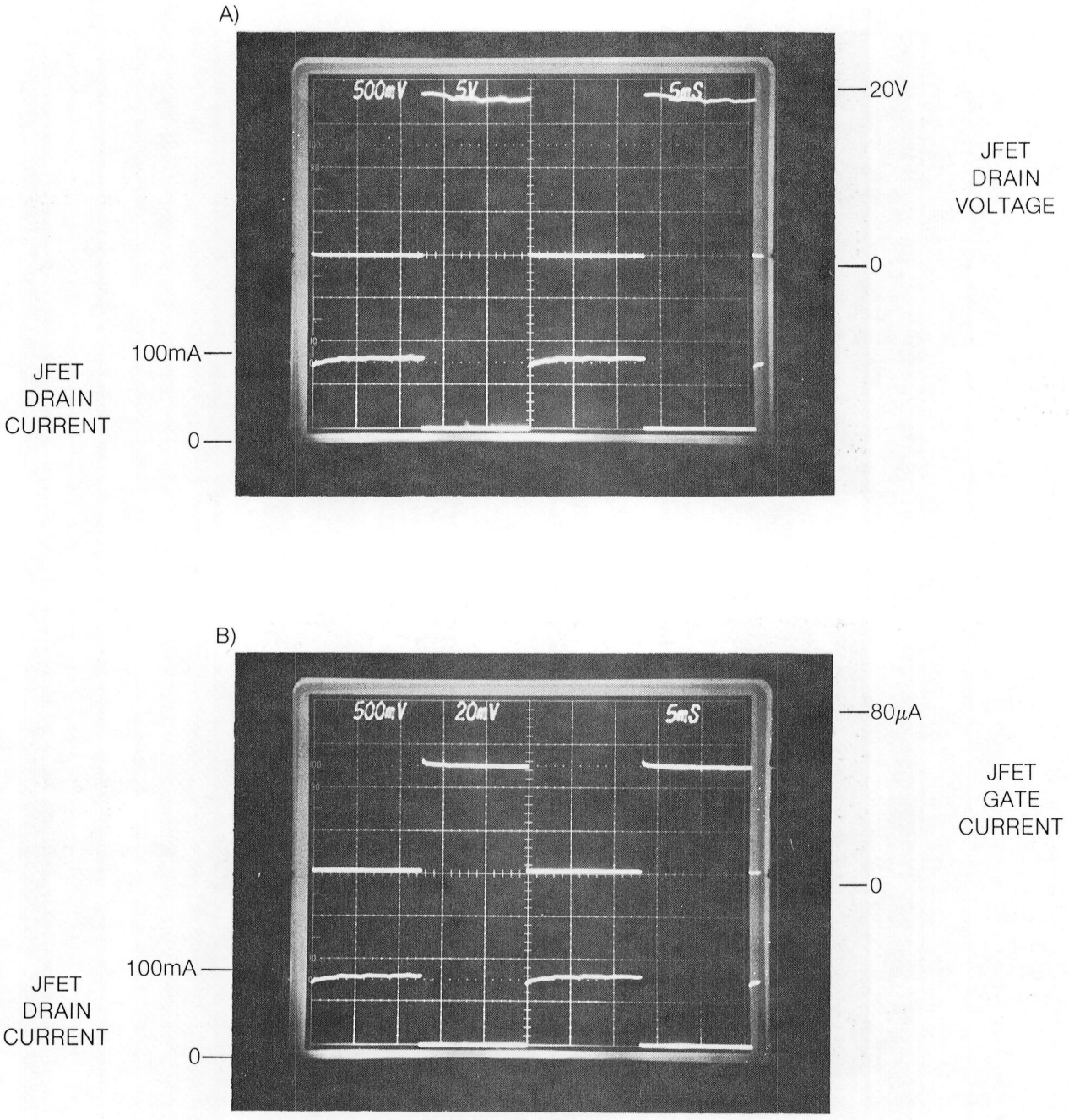
JFET drain voltage and current as well as gate leakage current at 253°C for Set B are shown in Fig. 6-2. When JFET gate voltage was switched to V_p, inductive current was shunted through the protection diode. The diode forward-bias voltage added to the JFET drain during the time interval of protection; the slight increase is shown in the upper trace of Fig. 6-2. This additional voltage (ΔV_D) will vary with circuit current, inductance, time, and temperature. Its temperature dependence is illustrated in Fig. 6-3, which shows for device Set B higher-resolution photographs of off-state drain voltage at the temperature extremes of measurement. An estimate of the time constant for the breadboard load is 2 msec. Maximum measured values for ΔV_D are shown in Table XIII for the three device sets for the breadboard conditions. The maximum voltage that could be added to the JFET drain at 80-mA operation for each temperature can be obtained from data as shown in Fig. 5-30. For diode D3s, the maximum possible values were 1.13V, 1.77V, and 1.92V for 253°C, 24°C, and -55°C, respectively. The maximum values observed on the breadboard were less than the maximum possible values due to the finite time of the breadboard switching transient. The operating JFET gate leakage current (Fig. 6-2) is at its highest during the off-state. For each device set, Table XIII lists values of $I_{G,off}$ which have been corrected for current flowing in the high-impedance probe. A device goal was to keep this leakage current lower than 100 μA at 250°C. The gate leakage current was observed to decrease about a factor of two for each of several 15°C temperature decreases from 250°C.

Another circuit parameter was the value of the on-state JFET gate voltage ($V_{G,on}$). This voltage was essentially the value of reverse bias existing across the illuminated phototransistor to supply the roughly 1.3 mA required by the breadboard circuit. As shown in Table XIII, this value is similar for the three devices at a given temperature but is temperature dependent. This voltage drop is less than the knee (saturation) photocurrents on the phototransistor current-voltage curves because the breadboard phototransistors were overdriven with 50% more light than was required to generate the required 1.3-mA photocurrent.

The operating values needed for optical power emission from the fiber inside the phototransistor package were 350 μW (Sets B and C) and 760 μW (Set A). From Table III it can be inferred that about 650 μW and 1400 μW, respectively, were coupled into the optical fiber at the IRED while the total optical emission of the IRED was about 20 times higher. The most accurate phototransistor photoresponse measurements were made at room temperature and near 250°C prior to hermetic sealing (Figs. 5-18 to 5-20). Extrapolation to -54°C (based on fully packaged measurements) showed that 180 μW and 250 μW of optical power would have been required at the phototransistor to generate a knee photocurrent of 1.3 mA. The excess optical power emitted by the IRED was

JFET PARAMETERS

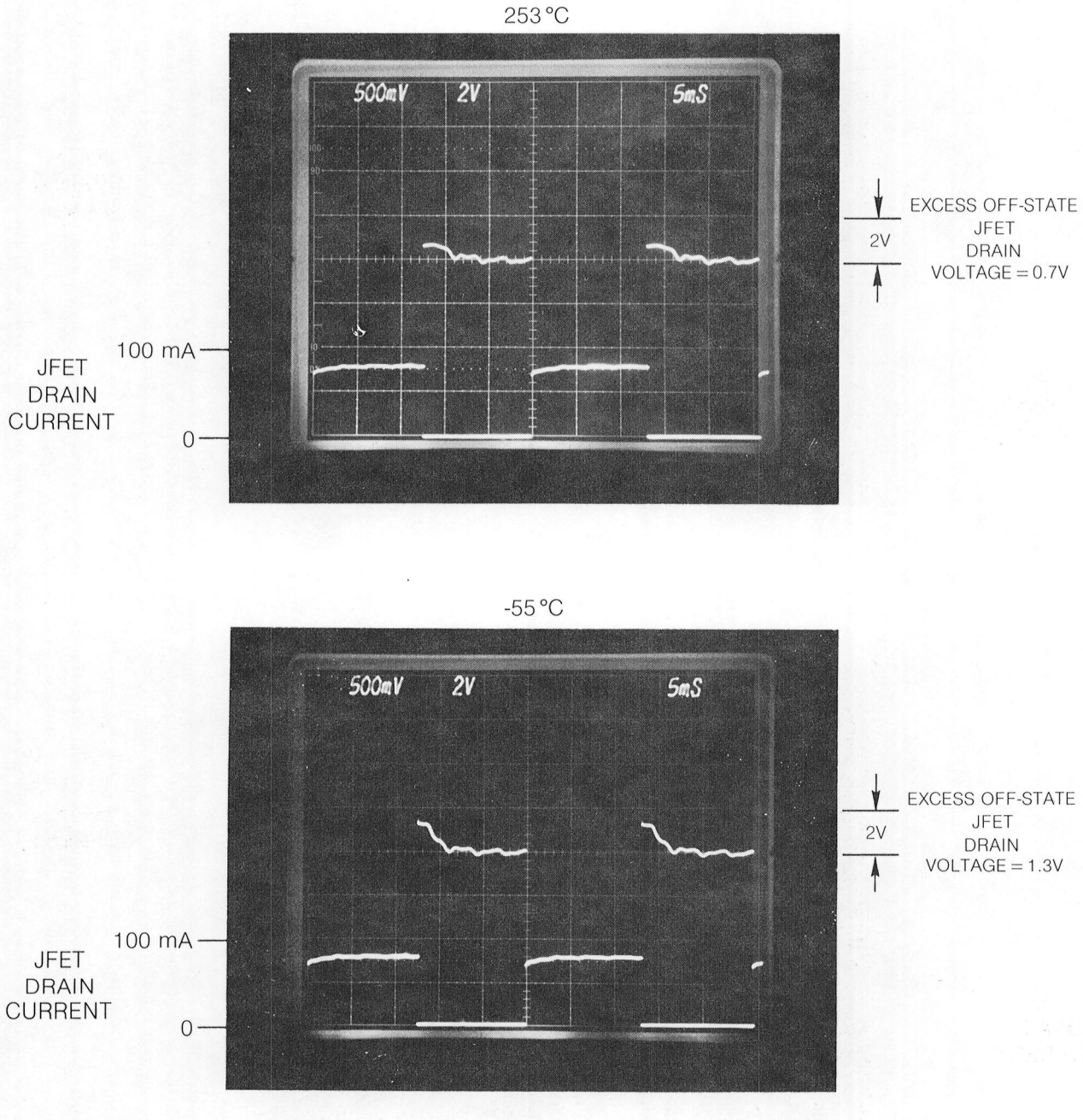
GaAs DEVICE SET B AT 253°C



82-10-9-1

JFET OFF-STATE DRAIN VOLTAGE WITH TRANSIENT PROTECTION

GaAs DEVICE SET B



83-3-119-32

either lost in coupling, fiber absorption, connectors, phototransistor coupling inefficiency or set aside for safety during breadboard operation. The phototransistors that survived to final testing and delivery were not those with the highest optical gain (see Table VIII and Figs. 5-10 and 5-11). If phototransistor K12d had been packaged, an expected 90 μW optical power corresponding to an optical gain of 30 would have been required to generate a knee photocurrent of 1.3 mA at -55°C. This is half the optical power requirements of phototransistors K11d and O13a. The advantage of using even higher-gain phototransistors is obvious. Further discussions of improved fly-by-light designs are given in the reported results of the study phase (Chapter 8.0).

PART II

FLY-BY-LIGHT POWER-BY-LIGHT FEASIBILITY STUDY AT HIGH TEMPERATURE

7.0 INTRODUCTION TO PART II

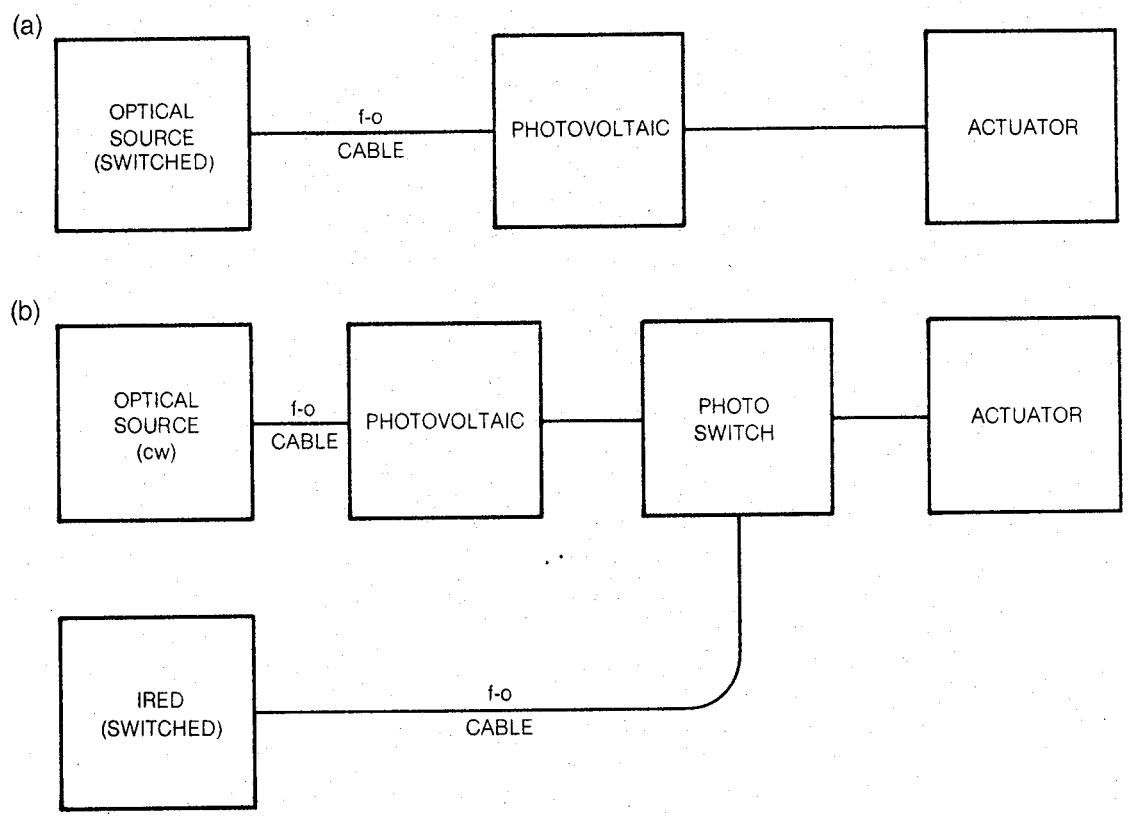
The objective of the Part-II add-on study program was to evaluate different schemes for utilizing optical energy to operate an actuator in high-temperature environments (up to 260°C). In Part I, a breadboard demonstration fly-by-light system was designed, fabricated and tested so as to permit control of electrical power using GaAs high-temperature devices which would operate between -54°C and 250°C. In Part II of this program improvements in this basic fly-by-light design are discussed. The major emphasis of the study program, however, was on power-by-light feasibility, specifically fiber optic transmission of optical power to a photovoltaic converter which would then supply the necessary electrical power to operate the torque motor. Important general areas of evaluation were system complexity and reliability, fabrication techniques, optical power budget and system power-conversion efficiency. The optical power source would be located at the control computer. The active photoswitch and/or photovoltaic devices would be placed at the high-temperature site near the actuator. Torque-motor operation could be controlled by using the pulse-width-modulated output of the control computer.

Two basic power-by-light systems are indicated by the block diagrams of Fig. 7-1(I). Both schemes require a high-power optical source, the output of which is converted to electrical energy by a photovoltaic cell or array of cells. In the first case (a), the control and power functions are combined, i.e., the optical power source is switched on and off in order to turn the actuator on and off. In the second case (b), an additional low-power optical source is used in conjunction with a photosensitive device to switch steady-state derived electrical power from the photovoltaic to the actuator. The system with the pulsed optical source is more efficient since the source is utilizing electrical power only when needed. It is also a simpler system to implement and is therefore preferred. High system efficiency is necessary for reduction of source optical and cooling requirements. Important factors in evaluation of a power-by-light system are shown in Fig. 7-2. Factors that must be evaluated are the efficiency of the optical path to the photovoltaic, the photovoltaic efficiency, and losses associated with impedance mismatch of photovoltaic with the load. In Fig. 7-2, a subscript has been used for the first four blocks due to the possibility of using multiple optical sources to

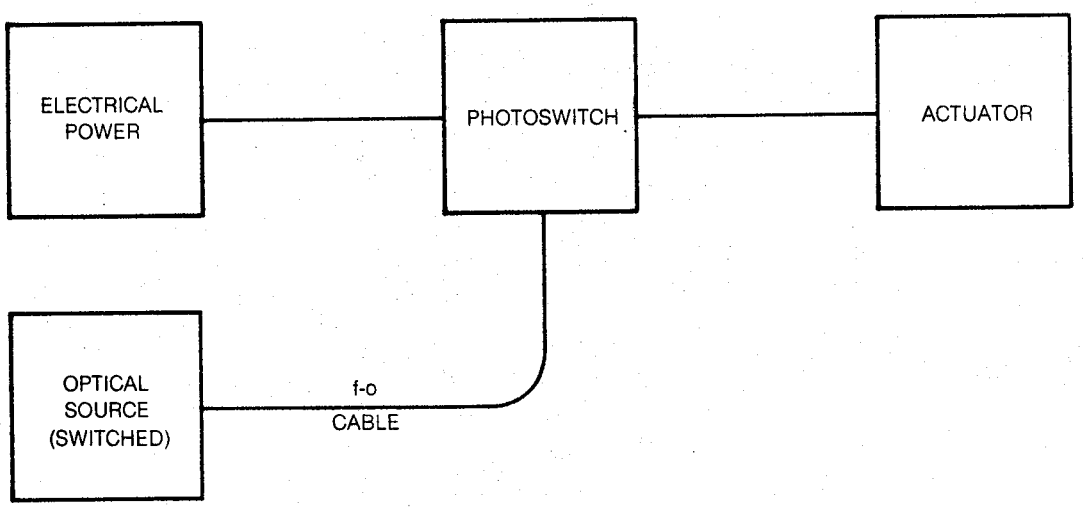
FIG. 7-1

CONFIGURATIONS FOR ACTUATOR OPERATION USING FIBER OPTICS

I. POWER-BY-LIGHT



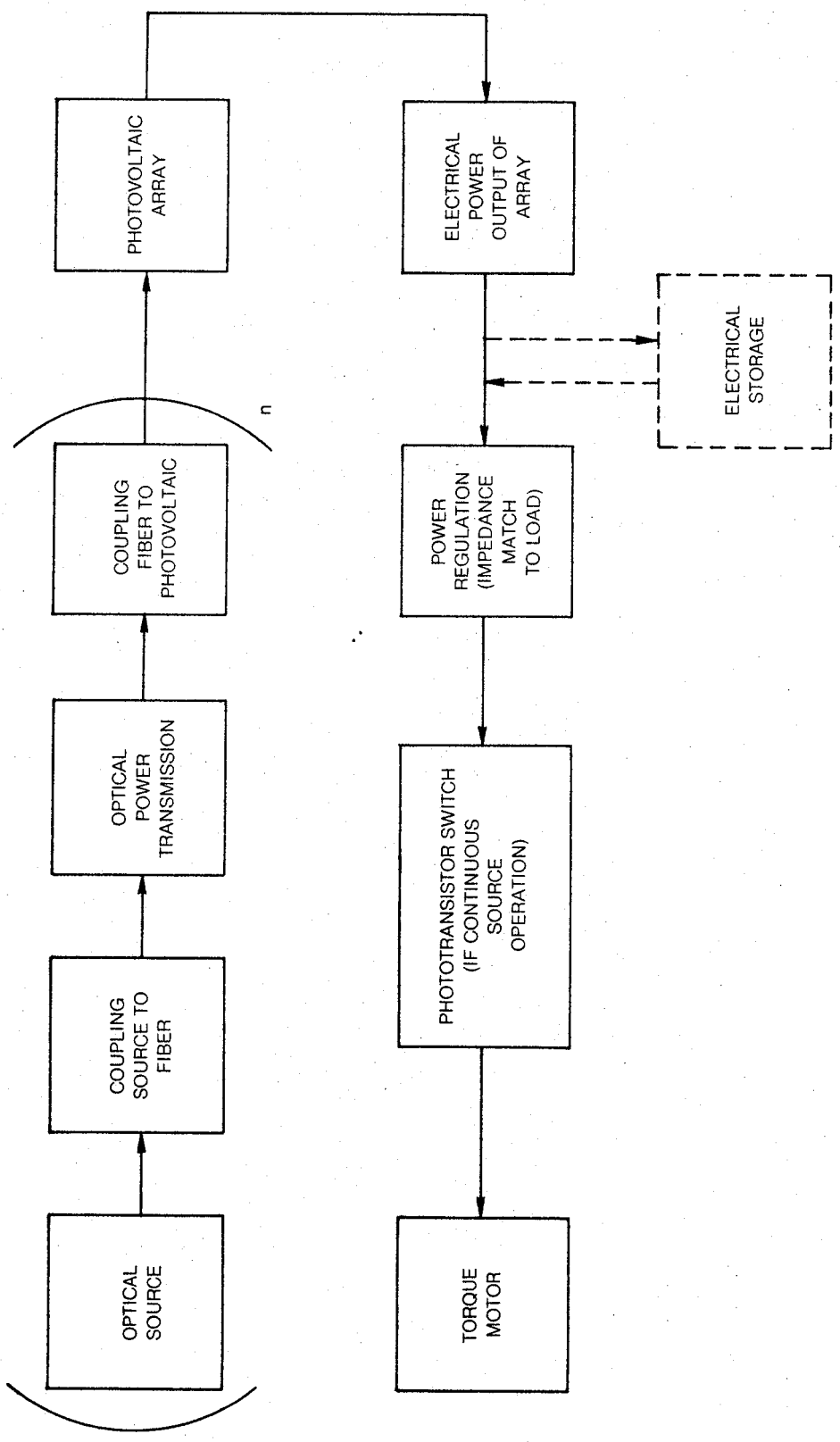
II. FLY-BY-LIGHT



82-6-43-2

FIG. 7-2

KEY SYSTEM FACTORS IN EVALUATION OF POWER-BY-LIGHT CONCEPT



82-6-43-3

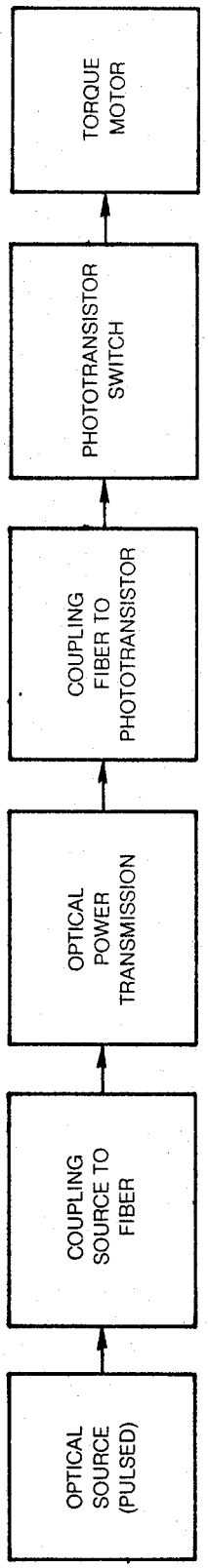
meet the power requirements of the actuator. For the case of cw operation of the source, there is the possibility of electrical storage of the photovoltaic output during the time the photoswitch has turned off power to the load. The constraint of operating in the -54°C to 260°C range is a severe one for an electrical storage system. Capacitor systems are inadequate due to low storage capacity. As a result of investigations into chemical storage during this program, there is no worthwhile battery system that could operate over the entire application range. Electrical storage has therefore been eliminated as a practical option in the rest of this report. The other factors in Fig. 7-2 have been evaluated.

The basic fly-by-light scheme is indicated in Fig. 7-1(II) in which electrical power has been assumed to be available from another source. In order to take full advantage of the fly-by-light concept, the electrical source should be located near the actuator. Only a photosensitive switch with a lower-power pulsed optical source is required to control actuator power. Similar evaluation factors (as in power by light) exist for the efficiency of optical power transmitted to the photodevice (Fig. 7-3). In a fly-by-light system, reduction in the optical power required to operate the torque motor is important to enable use of lower-power solid-state IRED sources. This can be done by maximizing the efficiency of the light path and gain of the photosensitive device.

Due principally to the higher band gap of GaAs compared to silicon, improved high-temperature performance will result with GaAs detectors and photovoltaics, and higher output voltage per cell will be obtained with GaAs. In order to match the optical source with the GaAs absorber, a source wavelength below about 8700Å at room temperature must be used. The closer the wavelength match of source to the GaAs absorber, then the higher is the system efficiency. Candidates for optical sources in power-by-light and fly-by-light configurations are semiconductor emitters, tungsten-halogen lamps and arc lamps. The lamps emit a wide spectrum of radiation in the ultraviolet, visible and infrared. The semiconductor devices emit in a discrete band of energy fixed by the semiconductor band gap. Several families of these are available including Group-III-V and IV-VI compounds in ternary and quaternary combinations. Of these, only those near 1.5-eV band gap, most notably Group-III-V GaAs emitters, would qualify in efficiency of emission and efficiency of detection. The available semiconductor sources are configured as light-emitting diodes or injection laser diodes (ILD). The applicability of each of these sources in fly-by-light and power-by-light applications will be discussed more fully in respective chapters of this report.

FIG. 7-3

KEY SYSTEM FACTORS IN EVALUATION OF FLY-BY-LIGHT CONCEPT



82-6-43-4

Several special factors enter into the choice of optical fibers for fly-by-light and power-by-light systems. Since the active devices must operate between -54°C and 260°C, the fiber core and cladding must be all glass. The usual materials that make up the outer covering will not survive the high temperature. In Part I of this program emphasis was placed on the performance of the GaAs devices especially at high temperature. In the packaging of phototransistors, the cable materials were stripped away so that only the glass fiber entered the high-temperature ambient. The same technique can be used for more advanced fly-by-light or power-by-light configurations. If optical cables could be made to withstand the temperature range of operation, then only that portion of the cable near the package seals would have to be stripped to expose the glass fiber. The brazing technique to seal glass fibers for high-temperature application requires that the fiber maintain its integrity at sealing temperatures between 300°C and 400°C. The glass fiber does not need to have ultra-low optical attenuation since for airborne applications the fiber lengths are short (<10 meters). The fibers should be multimode and have high numerical aperture to couple as much optical energy into the fiber as possible. Very high bandwidths are not required since anticipated frequencies used for aircraft control will be less than 2 kHz and again the lengths are short. For increased coupling to the IRED, large core diameter (200 μm) and high fiber NA (0.4 to 0.55) are required. Edge-emitting devices (e.g., ILD) can efficiently couple to smaller diameter fibers. Much larger glass core diameters (1000 μm) could be used for coupling to the lamps.

Optical connectors on the pigtails are used together with a transmission fiber and connectors in order to facilitate replacement of either the source or photodevice if need be. The optical transmission loss can be separated into fiber loss and connector loss. Fiber loss includes dB/km loss as well as effective reduction of the numerical aperture for lengths in excess of about 200 meters. This latter factor is not important for airborne applications. Calculations of coupling and transmission losses will be given in subsequent chapters for specific cases.

When considering coupling of optical fiber(s) to the photodevice, two important questions arise: (1) What coupling techniques should be used to maximize the area overlap of light emerging from the fiber(s) with the device active area? (2) How should device packaging be implemented to insure long-term reliable operation from low (-54°C) to high (260°C) temperature? UTRC device packaging experience for high-temperature operation has been exclusively concerned with mating a single source with a single fiber with a single photodevice in a single package. Increasing the number of fibers to be hermetically sealed in a package will result in considerably more difficulty and lower packaging yield.

Independent of the optical source, single-fiber emission will have circular symmetry. In order to maximize the area overlap of light emerging from the fiber with the photodevice area without introducing the additional complexity of lenses, the photodevice diameter must be at least as large as the fiber-core diameter, or correspondingly larger if a fiber array is used. Ideally, the incident optical energy should be uniform and entirely blanket the photosensitive area without spilling outside the device. Necessary metallization on the photodevice active surface will reduce overall device efficiency. The numerical aperture of the optical fiber requires close placement of the end of the fiber above a given photodevice area. Actual contact is not recommended due to possible damage of fiber or device, especially during temperature cycling. Unless the flat end of the fiber is anti-reflection coated there will be about a 4% light loss at the glass-air interface. The fiber tip should be well polished to a specular surface using a grit diameter less than the intended wavelength (~ 8200Å) in order to minimize scattering losses. The photosensitive device should have an anti-reflection coating to reduce the 30% reflectivity of the GaAs surface to more acceptable values (less than a few percent).

The photovoltaic or photodetector has to be packaged to withstand temperature cycling between -54°C and 260°C and long-term operation at 260°C. Mating of an optical fiber with a photodevice severely affects the packaging procedure not only because of fiber-device positioning requirements but also because of the need for preservation of long-term device hermeticity while operating in high and low-temperature ambients. Hermetic device packaging is very important for GaAs because there is no satisfactory passivating material available for GaAs as there is for silicon devices (SiO_2). Exposed GaAs p-n junctions and surfaces should be protected from any environmental influence, e.g., particulates, O_2, H_2O, or other reactive gases. Use of high-temperature epoxys has been avoided principally because of possible high-temperature outgassing of contaminants from cured epoxy within the package that could degrade device performance. Instead, technology to hermetically seal glass optical fibers using cleaner brazing techniques for more reliable and longer-term device operation has been applied to phototransistors packaged in Part I of this program.

In the next two chapters the factors entering into the block diagrams of Figs. 7-2 and 7-3 will be quantified for various practical cases. The fly-by-light study effort ended with suggested configurations which represented next levels of advancement compared to the system delivered in Part I. At the end of the power-by-light study, a demonstration configuration was recommended for future work.

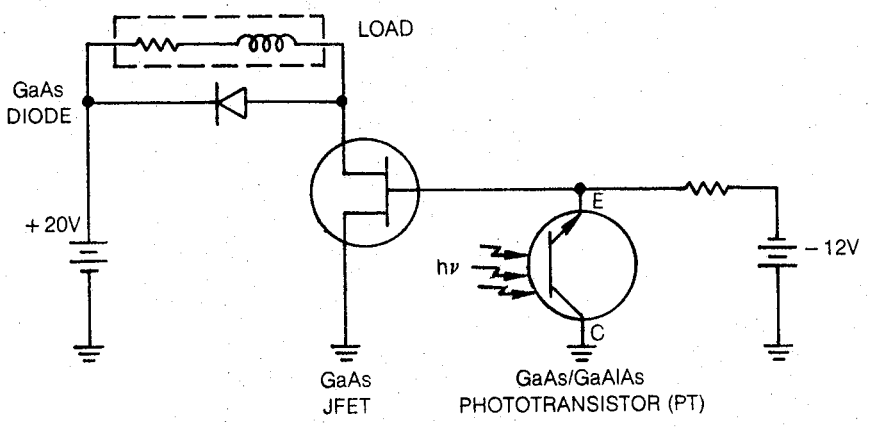
8.0 FLY-BY-LIGHT DESIGNS AND DISCUSSION OF RESULTS

The high-temperature fly-by-light system delivered in Part I of this program utilized three GaAs-based devices. The phototransistor was the light-sensitive element (which also exhibited gain) that caused a higher-power JFET device to switch current into the torque-motor load. A third device, a p^+-n mesa diode, was placed across the load to protect the JFET from inductive transients. As shown in Fig. 8-1A, the phototransistor was placed in parallel with the JFET gate to provide torque-motor actuation when illuminated. The system was capable of switching 100 mA at up to 20V stand-off voltage (2W into load) with from 240 μW to 510 μW (350 μW - 760 μW recommended) of infrared radiation exiting the optical fiber inside the sealed phototransistor package. For the recommended breadboard operation, 650 μW to 1400 μW had to be coupled into the optical fiber. Group-III-V GaAs solid-state sources are ideal for fly-by-light application because (1) optical emission is at the proper wavelength and of sufficient power using a single optical fiber for phototransistor operation, (2) lifetime is in excess of 10^4 hours, and (3) the sources are readily pulse-width modulated. The temperature range of application for the photoswitch devices was -54°C to 250°C. This could have been extended to 260°C with slight increase in required optical power. There are two avenues of advancement using GaAs devices in the -54°C to 260°C range. The first is to be able to switch significantly more current into heavy-duty torque motors or centrifugal motors, and the second is to simplify the photoswitch circuit and provide greater reliability for switching moderate-to-low currents (less than about 200 mA).

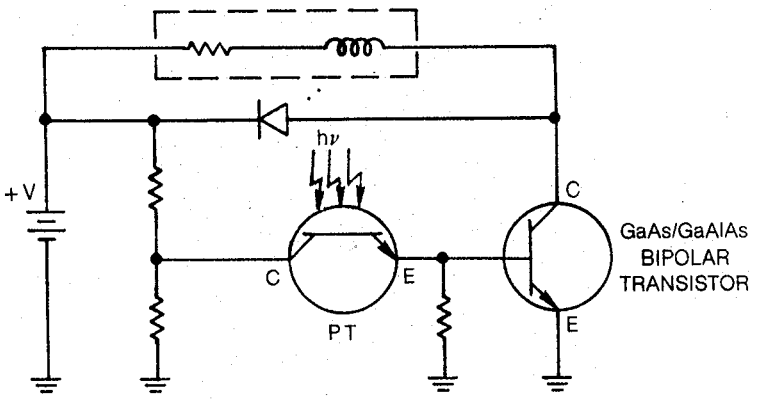
Higher-power switching could be accomplished with the delivered fly-by-light system by either increasing JFET stand-off voltage or current capability. The latter approach would require increasing the gate width and therefore, area of the device. One criticism of the JFET for high-power switchng is that this device conducts parallel to the surface in a thin surface layer rather than perpendicular to the device as in, for instance, a bipolar transistor. As a result JFET device resistance, area and leakage currents will be higher for a given switching level. Furthermore, JFET performance is more highly affected by surface instabilities. Since a suitable surface passivant is not yet available for GaAs, this is an important factor. Higher leakage currents that accompany a scaled increase in JFET device size would be accommodated in Fig. 8-1A by forcing the phototransistor to become more conductive during the on-state, that is, supply increased optical energy or phototransistor gain. The GaAs JFET will probably not be useful for switching more than about 1 ampere at 260°C. Also, JFET stand-off voltage is not expected to be above about 20V at this temperature without adequate surface passivation.

FLY-BY-LIGHT CONFIGURATIONS USING GaAs BASED DEVICES

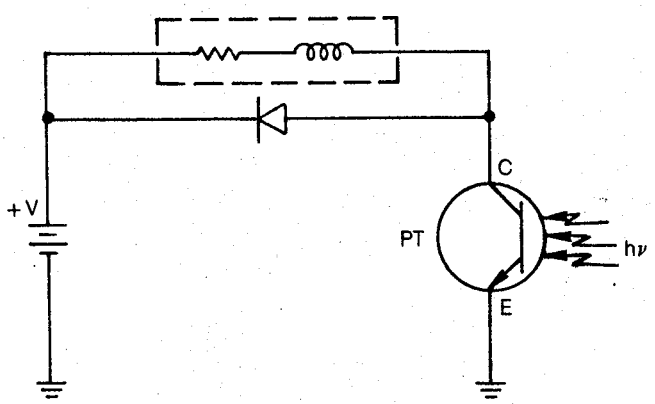
A)



B)



C)



82–11–70–2

For fiber optic control of electrical power above 10 to 20 watts, use can be made of a GaAlAs/GaAs bipolar transistor or a GaAs permeable-base FET. A VMOS or VMIS device requires a passivating insulator layer which can be used to invert the semiconductor material underneath; however, the proper insulating material has not been demonstrated for GaAs. The permeable-base Schottky Barrier FET incorporates a buried metallic grid which is used to gate current flow through to the substrate. Such a device (or its p-n junction analogue) is very difficult to fabricate and needs further development especially for high-temperature use.

A promising candidate for higher-power switching is the bipolar transistor. This device is constructed layerwise in much the same way as the n/p/n (bipolar) phototransistor (Fig. 3-1) in the delivered breadboard system. In the case of the phototransistor, the upper GaAlAs layer is a window for the incident radiation and is highly efficient at injecting electrons into the p-type base. The bipolar transistor utilizes the GaAlAs to provide the same high injection efficiency but optical transparency is not required. Both devices require a thin base layer for high gain. The phototransistor can operate with base floating (2-terminal device). The bipolar transistor requires contact to the thin base and is, therefore more difficult to fabricate. For high-temperature application, the design must be such as to eliminate metal contact diffusion and degradation of the base-collector junction. As shown in Fig. 8-1B, photocurrent generated in the phototransistor (PT) could be used to operate a high-current-capability bipolar transistor. In the literature, current gains near or in excess of 1000 have been reported for the GaAs/GaAlAs bipolar transistor at high injection levels (Refs. 8 and 15). In Ref. 15, room temperature saturation currents in excess of 300 mA have been reported for devices having an area of $1 \times 10^{-4} cm^2$. It is interesting to compare these values with saturation currents for typical JFET's like those used for the breadboard photoswitch system. A typical JFET saturation current was 500 mA -600 mA (-11 to -13V gate) but the active region was about 12 times larger than the referenced bipolar device. Thus, the maximum current density is at least a factor of 6 better for the bipolar device. One reported operating point was 60 mA of collector current with 100-μA base current. At this point 2.7V were dropped across the emitter-collector terminals. If the device area were scaled by a factor of 100 to $1 \times 10^{-2} cm^2$ to conduct 6A with a 10-mA base current, 16 W would be dissipated across the device. If the power supply voltage were 15V, then 74 watts could be switched to a load. This illustrates one disadvantage of bipolar devices compared to FET's and that is the relatively large internal power dissipation. One problem with extrapolating bipolar device characteristics to larger sizes for a given base thickness is that base resistance effects will cause a reduction in point-to-point base current density as the distance from the contact increases; therefore, important factors in design include base thickness, carrier concentration, carrier mobility, and contact geometry and

metallization. Fortunately, the wide-gap emitter will inject electrons into the base at very high efficiency regardless of majority carrier concentration on either side of the heterobarrier. Thus, unlike the case of a silicon transistor, the GaAs base can have a higher doping level than the emitter, and base resistance can be minimized without a loss in injection efficiency.

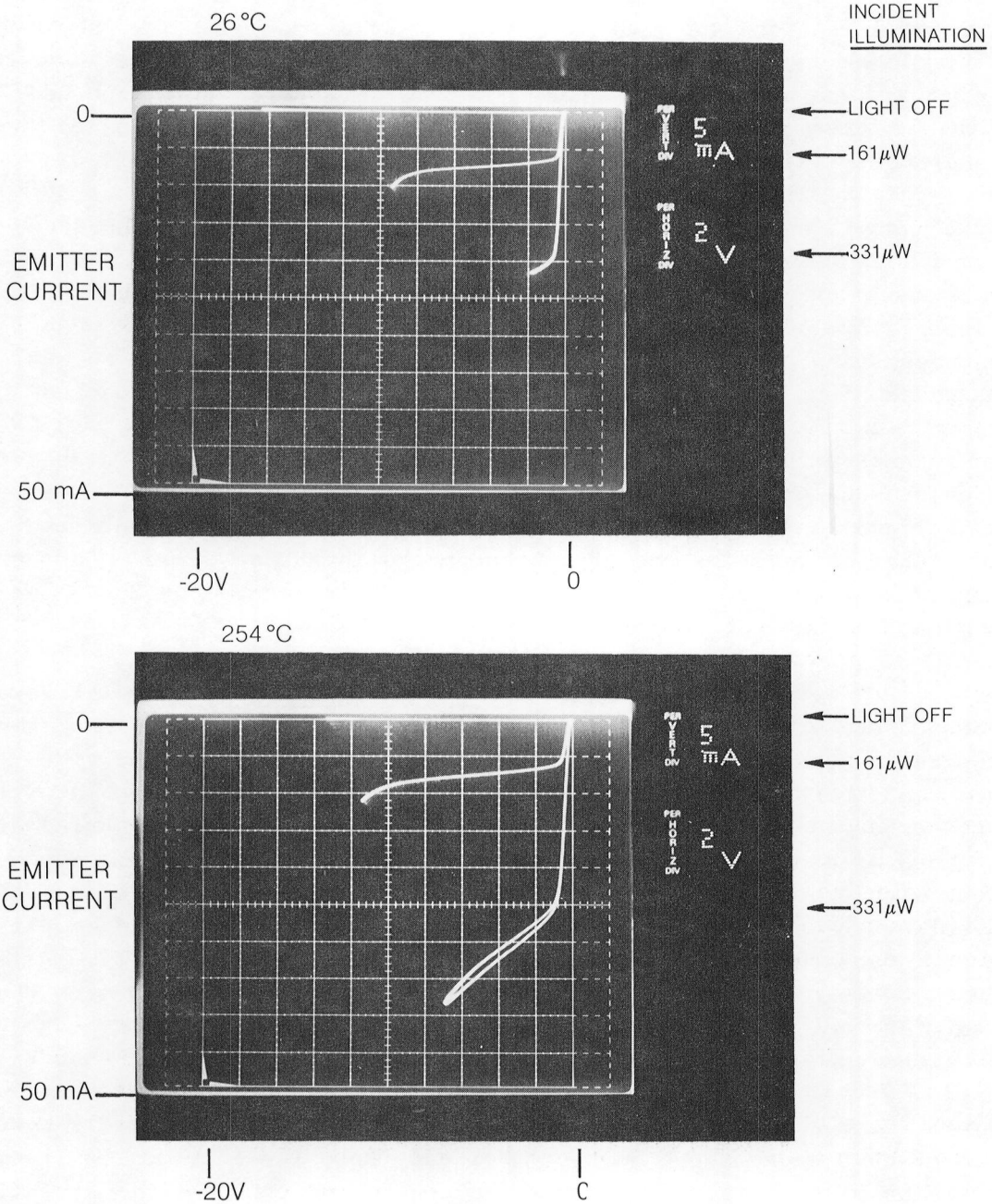
The circuit configuration in Fig. 8-1A can be simplified for switching moderate currents by replacing the JFET-phototransistor pair with a single phototransistor having higher optical gain. Figure 8-1C illustrates the simplicity (and consequently greater reliability) of the circuit configuration. Phototransistor gain can be increased by decreasing the base thickness. Optical gains for p^+-base devices at high-injection levels have been reported in the range, 100 to 200 (Ref. 6). For devices made at UTRC, optical gains in this range have been measured. As evidenced by the referenced bipolar transistor work, the optical gain, which takes into account device quantum efficiency, should be substantially higher with thinner p^+ bases. An extraordinarily high optical gain (about 5000) has been reported for a phototransistor having a thin base with low p-type doping (Ref. 16). (Since the phototransistor operates with base floating, there is no need to worry about lateral base resistance as in the bipolar transistor.) The phototransistor with low-p base relies on depletion-layer spreading into the base layer for enhanced gain. Although reported room temperature photocurrents were quite high (500 mA), the dark current was also high (30 mA at -5.5V). Since 4V were dropped across the phototransistor, available power to the load was only 0.75W (1.5V at 500 mA). This device is more suited for high-current low-voltage switching. The lower-gain p^+-base devices can support -15V emitter-collector voltage in the off-state; however, increasing the device gain will cause this voltage to decrease.

Phototransistor gain can also be increased by increasing the intensity of illumination. A commonly observed property of GaAlAs/GaAs bipolar devices is that defect currents exist at the hetero-interface and their relative influence on device gain decreases as the injection level increases. There is, therefore, the option of operating lower-gain devices at high optical power densities using a laser diode. An optical power of 20 mW can be readily supplied to a photosensitive device using a single fiber optic line and an injection laser diode. If reference is made to plots of phototransistor knee photocurrent versus illumination for fully packaged p^+-base devices (see, for example Fig. 5-18), over 0.2A of photocurrent would be expected at 20-mW optical power. Device power dissipation would increase to perhaps 2V x 0.2A or 0.4W. If the maximum useful collector voltage were -15V, then 2.6W would be available for the load. Figure 8-2 shows pre-packaging current-voltage characteristics of that phototransistor with the highest gain observed in Part I of this program. (Other data were shown in Figs. 5.5 and 5-7.) It is not

PHOTOTRANSISTOR CURRENT-VOLTAGE CHARACTERISTICS (K12d)

BASE FLOATING-COLLECTOR GROUNDED

$\lambda = 8499\text{Å}$



83-3-119-30

difficult to extrapolate operation of this device to 200 mA at higher incident optical powers. Phototransistor operation at high current levels may require a device with larger diameter than 200 μm in order to reduce internal power dissipation. This would require that more optical power be supplied to maintain the same optical gain.

The optical path to the phototransistor consists of source with fiber optic pigtail, optical connector, transmission cable, optical connector and fiber optic pigtail to the phototransistor package. A summary of power transfer efficiencies for the two types of solid-state diode sources is shown in Table XIV. These devices were chosen for fly-by-light (as well as power-by-light) applications because they were commercially available high-power sources and emitted radiation at the proper wavelength for matching to the phototransistor. This type of ILD (60-μm-stripe width) can be driven to emit over 100 mW per facet with a resultant power-converson efficiency of 30%; however, longer-life operation (up to 10^4 hours) is possible at the 60-mW per-facet level (19% power-converson efficiency). The ILD calculations of Table XIV were based on single-fiber coupling to one ILD facet without back-facet coating; therefore 50% of the emitted optical power was not usable. An important operating characteristic of this high-power ILD is that to preserve lifetime the ambient temperature has to be less than 35°C. An expected increase in lifetime by one order of magnitude would accompany each 30°C decrease in heat-sink temperature. The chosen IRED is a slightly higher-power version of the one used in the Part-I breadboard demonstrator. This device is a planar surface emitter with a transparent GaAlAs dome for greater fiber coupling efficiency. It is specified to operate in excess of 10^5 hours at dc drive currents under 200 mA before optical output is reduced by 20%. The operating maximum ambient temperature is 65°C for this IRED.

The primary factors governing efficiency in coupling multimode fibers to these sources are area overlap and angular overlap. The area overlap simply involves getting the light into the fiber core with whatever angle of incidence, and the angle overlap involves that portion of the light arriving at the proper angle to be within the NA of the fiber. The butt coupled ILD has very good area overlap with the fibers but the 3:1 astigmatism, which is due to the high width-to-thickness ratio of the diode junction, degrades the angle overlap. Because of the lower NA's and consequently reduced coupling efficiency, standard 62-μm-core fibers were not listed in Table XIV. A lens can be used to magnify the laser-diode emitting region. This improves the angular overlap but could only be used with a larger-diameter core, e.g., 200 μm. Any technique used to magnify the laser-diode facet will decrease the area overlap with a 100-μm fiber because the 60-μm and 100-μm areas were already well matched. Two known astigmatic techniques are applicable here. One is to grind a wedge shape on the fiber end (Ref. 17) so that the laser-diode emission pattern is split across the center and each half is moved to produce an increased angular overlap in the fiber. Likewise, a small cylinder

TABLE XIV

OPTICAL POWER-TRANSFER EFFICIENCIES USING SOLID-STATE SOURCES AND SINGLE FIBERS

Source	Electrical Power Input	Device E → O (%)	ILD*** Efficiency (%)	Fiber Coupling Efficiency (%)	10-Meter Transmission Efficiency (%)	Two-Connector Transmission (%)	Overall Efficiency (%)	Fiber Output (mW)
ILD*	320mA-2V	19	50	40 (100,0.3)†	98	50	1.9	12
				60 (100,0.55)	97	50	2.8	18
				75 (100,0.55,w)	97	50	3.7	24
				80 (200,0.55,w)	97	63	4.6	30
IRED**	200mA-1.6V	17	--	4.3 (200,0.55)	97	63	0.44	1.4

* λ = 8200Å, 35°C Maximum Ambient Temperature
** λ = 8360Å, 65°C Maximum Ambient Temperature
***ILD Back Facet is Not Coated

† (Fiber core diameter, fiber NA)
w = wedge-end polished optical fiber

lens can accomplish the same thing by magnifying the diode junction thickness (about 1 μm) without affecting the 60-μm width. IRED coupling has both poor area overlap and poor angle overlap, at least for the large-area device being considered, and little if any power coupling efficiency can be gained with fiber lenses. For the selected IRED, redirecting the emitted optical energy for fiber coupling is an integral part of the device. Butt coupling of the fiber is therefore preferred. For higher-efficiency IRED coupling, a high-NA large-diameter 200-μm fiber should be used.

The efficiency of transmission of the near-infrared radiation through the optical fibers is high for the short cable lengths contemplated in aircraft control applications. Connector loss for standard purchased connectors has been conservatively set at 1 dB and 1.5 dB for 200-μm and 100-μm-core diameters, respectively. These are maximum anticipated losses; the range of commonly observed experimental values can be as low as one-half these values.

The overall efficiency of optical power generation and transmittal can be as high as 4.6% for the ILD case but is ten times less for the IRED. Up to about 1.4 mA of optical power (IRED) and 30 mW (ILD) can be obtained as fiber output for the phototransistor. Depending on phototransistor surface reflectivity, distance from the fiber, fiber NA and diameter, and phototransistor diameter, the actual usable optical power will be less. The IRED source can be used with either a high-gain phototransistor to switch large currents at low voltage or with low-gain devices for lower-current switching at higher voltages. The injection laser diode could be used with low-gain devices to switch higher powers. When applicable it is best to use the IRED in a particular application for ease of use, longer life, and less expense.

In conclusion, higher-current switching under fiber optic control can be accomplished by using higher-gain phototransistors and/or higher illumination levels from a laser diode. Phototransistors can be constructed with low or high p-type base doping to produce (1) high-gain devices with deliverable power of about 1W for low-voltage application or (2) lower-gain devices switching less current but at higher voltage. The highest switching power under fly-by-light control can be obtained with a bipolar transistor triggered by the phototransistor. Considerable decrease in circuit complexity and therefore, increase in system reliability can be achieved by replacing the JFET-phototransistor pair with a single phototransistor. Any of these options are candidates for future work. The transient-protection diode is still required for an inductive load, which may be a torque motor or centrifugal motor.

9.0 POWER-BY-LIGHT FEASIBILITY AND DISCUSSION OF RESULTS

In accordance with the outline for power-by-light evaluation given in Fig. 7-2, this section is divided into discussions on optical power generaton and delivery to the photovoltaic device, photovoltaic device design, photovoltaic power-conversion efficiency, and photovoltaic impedance matching to the torque-motor load. After discussion of these factors, a power-by-light demonstration system is proposed for use over the -54°C to 260°C temperature range using GaAs semiconductor devices. Suggested areas for additional work are presented in the last section of this chapter.

9.1 Optical Power Delivery to the Photovoltaic

The approach followed in this program on fly-by-light designs has been to use GaAs solid-state optical sources that emit at wavelengths which match the characteristics of the absorbing GaAs device (phototransistor). In such control situations the photoswitch device acts as a switch for externally supplied electrical power for the torque motor. The required optical power depends on circuit configuration (i.e., presence of an additional switching device and how it is connected to the phototransistor) and phototransistor gain. The fly-by-light optical requirements can be met using either an IRED (preferred) or an ILD with a single fiber optic channel. Because of their long lifetimes and ready applicability to pulse-width modulation, these sources are natural candidates for fly-by-light control, even if cooling is required to keep the ambient temperature of present-day sources to less than 65°C (high-power IRED) or 35°C (high-power ILD). One way to cool these devices would be with thermoelectric coolers which would require two stages (25% efficient) for the IRED and 3 stages (12% efficient) for the ILD.

In the power-by-light concept, all necessary electrical power for the torque motor must be supplied first as optical power which is then transmitted to the photovoltaic converter. As was shown in Table XIV for the solid-state sources, optical generation, coupling and transmission exact a heavy toll on system efficiency. As will be shown later, system efficiency is reduced considerably further by the photovoltaic and its degree of impedance matching to the load. For the solid-state sources, a smaller number of f-o lines is required to transmit a specified optical power using an ILD due to its highly directed optical emission (more efficient fiber coupling). In order to optically generate sufficient electrical power for the torque motor, many sources and fiber optic lines would be employed, and the transferred light would be incident on an array of photovoltaic cells.

An alternative way of supplying optical power to the photovoltaic array is through use of high-intensity arc or tungsten-halogen lamps. Due to their relatively broad spectral emission, the lamps are not as well matched to the GaAs photovoltaic as the solid-state sources. In order for these extended sources to compete with the efficiency of fiber coupling to a laser diode, the use of a fiber optic bundle for each lamp is required. A single lamp is much less expensive than many laser diodes but other cost and performance factors must be considered. For instance, the lamps have significantly shorter lifetime compared to the solid-state devices. Estimated source lifetime for high-intensity arc and tungsten-halogen lamps are 100-500 hours and 50-300 hours, respectively, compared to 10^4 hours for the ILD and 10^5 hours for the IRED. As far as overall system efficiency is concerned, the lamps would have to be operated in a cw fashion in a power-by-light application. Solid-state semiconductor diodes can be rapidly pulsed on and off, and therefore, are readily adaptable to efficient pulse-width-modulation control on aircraft. Arc lamps cannot be pulsed off rapidly enough. For reasonably short pulse widths tungsten lamps would have to be electrically overdriven with a smaller filament but this would degrade lifetime even further. Xenon flash lamps typically produce pulses much shorter than are usable in a pulse-width modulation system and are limited in lifetime to 10^6 to 10^9 pulses. In order to use the lamps, optical chopping using a photoswitch would be required in the torque-motor circuit (Fig. 7-1, Ib). As a result, an additional efficiency factor (~ 5-50%) relating to duty cycle and complexity factor for the extra fiber optic line and electrical circuitry should be considered when making comparisons to the semiconductor sources.

Of significant concern in usage of lamps is the considerable energy in the form of heat which must be dissipated to assure continued lamp operation. While the I^2R heat removal problem is readily addressable when solid-state sources are used, there is greater difficulty in deriving a system penalty for cooling purposes in the case of the lamps if these were to be used as aircraft power-by-light sources. A typical high-intensity lamp operated at room temperature requires either forced air or forced liquid cooling. To be useful in a 125°C ambient, additional cooling would be required. Liquid cooling is indicated especially in view of the rarified atmosphere which accompanies an altitude increase. As a result, assessment of a cooling penalty factor for the lamps is highly dependent on lamp design and system configuration. Other factors with lamps are susceptibility to catastrophic demise (explosion) and lamp orientation, especially for arc lamps. Another consideration is the optical-source power supply. The least complicated supply would be required for a tungsten-halogen lamp; the most complicated would be for the arc lamp to provide both high-voltage ignition and low-voltage dc during operation. Unwanted arcing can also be a problem at high altitude for the high-voltage power supply.

Efficiency calculations similar to those in Table XIV have been made for representative commercial arc and tungsten-halogen ($W\text{-}X_2$) light sources. Compact short-arc high-pressure-xenon illuminators are available with a built-in reflector (2.5-cm diameter) to supply a near-parallel light output. These emit principally broadband radiation in the visible and infrared and have an estimated lifetime of 300 hours at rated power. Two $W\text{-}X_2$ sources, presumed to have a black-body temperature of 3200°K, were studied. Further calculations have also been made for the GaAs solid-state sources. Except for the ILD, coupling of optical energy from any of these sources into a single fiber is highly inefficient because of the large-angle emission. To maximize efficiency, a lens system must be used to collect as much light as possible from each source and focus it to within the numerical aperture of a fiber bundle. Source magnification accompanies angular demagnification, and therefore, the size of the fiber bundle will depend on fiber NA and spatial extent of the source. Such an arrangement will require a large number of closely packed fibers. Coupled optical power will increase with the degree of close packaging of the fiber cores. The number of required fibers will decrease as core size increases at constant NA. In the calculations made, two fiber types were utilized: (1) a soft-glass fiber with a core diameter (d_c) of 200 μm and an NA of 0.55 (as used in the hardward phase of this program) and (b) a fused-quartz fiber having a d_c of 1000 μm and an NA of 0.3. The latter fiber will be considerably more expensive than the former and have less mechanical flexibility. The large-core fiber will couple more optical power but the optical energy carried per cross-sectional area of fiber will be larger for the higher-NA fiber.

Due to the highly directional emission of the laser diode, coupling of one fiber to each ILD facet is efficiently made with specially polished fibers (Table XIV). A build-up in optical power at the photovoltaic requires the use of additional laser diode sources, each with one or two coupled optical fibers. The individual fibers can be collected and distributed at the photovoltaic array. In contrast, each lamp and IRED will utilize a bundle of coupled fibers. The simplest system would involve close packing of each fiber bundle at a single photovoltaic cell. A more difficult and complex arrangement would be to partition the fibers at the photovoltaic array.

Table XV (in two parts) summarizes calculated system efficiencies for the selected sources. The focus of this chapter section is on Category I, Optical Power Generation and Delivery to GaAs Photovoltaic. Reference is also made to related comparisons in Category IV. Other categories will be discussed in Section 9.3. Electrical power utilized for the source power supply and source cooling were not included in Category I of this table.

The optical emission of the solid-state sources (Item I.A of Table XV) was set at 8200Å. An 8250Å upper wavelength limit was required as a result of the anticipated position of the GaAs photovoltaic absorption edge at -55°C. This absorption edge will move to about 8700Å at room temperature and 9130Å at 260°C as the GaAs energy band gap decreases. An interesting consequence in the case of the lamps is that a greater percentage of the optical power output is utilizable by the GaAs photovoltaic at higher temperatures. The efficiencies for electrical-to-optical output for the lamps for photon energies in excess of the GaAs band gap were obtained from manufacturer's specifications or through use of a black-body slide-rule calculator. Useful lamp output therefore increases by about 33% for photovoltaic temperature increases from -55°C to 260°C.

In Item I.B.1, the efficiency of optical coupling for the lamps was calculated using a reflector and/or an additional lens for angular demagnification of emitted optical power to within the acceptance angle of the fibers. The greater coupling efficiency for the close-packed array of larger-diameter fibers reflects an assumed larger area fraction of core to core-plus-cladding for the larger fiber. The diameter (d_t) of the clad soft glass fiber was 250 μm; the assumed value of d_t for the fused quartz fiber was 1111 μm. It was also assumed that the glass fibers were in contact for light coupling with no intervening jacketing materials present. The beam area or spot size (I.B.3) is smallest for the ILD, considerably larger for the IRED, and much larger for the lamps. The fiber bundles required for the IRED and arc lamps were close packed into a circular array; a rectangular close-packed array was used for the coiled-filament tungsten-halogen lamps. The number of optical fibers in the bundle is given in Item I.B.2 and can vary from several tens to several thousands for the chosen lamps. There will also be a nonuniform distribution of light intensity within the beam area. This is of little concern for power-by-light in the case of the ILD since only one fiber is butt coupled to a particular facet. In the other cases there will be a distribution of coupled optical power across the fiber bundle. This is especially true in the coiled-filament tungsten-lamp case and places restrictions on the way the fibers are combined at the photovoltaic. The advantage of using the much-brighter are lamp rather than a comparable-wattage tungsten-halogen lamp is clearly shown by comparing the spot size and number of fibers. Another concern is that unless a dichroic reflector is used for the lamps, longer-wavelength photons will be focussed onto the fiber array and possibly melt the soft-glass high-NA fiber or any other material used to hold the fiber array together.

The room-temperature optical power transmission of usable source emission over a 10-meter path is shown in Item I.C for the two fiber types. Optical attenuation data for the soft glass as well as for fused quartz (Ref. 18) were used to calculate a power transmission factor. Fiber attenuation increases as

wavelength decreases from the near infrared. The ultraviolet portion of lamp emission was highly attenuated even over a 10-meter path length. Attenuation in the soft glass is greater than for the fused quartz. The connector loss (I.D) assumed that each fiber-optic line had individual connectors, one at the source and another at the photovoltaic.

The totals for efficiency of usable optical power generation and delivery to the GaAs photovoltaic and coupled optical power into the fiber array are shown in Item I.E of Table XV. On the basis of efficiency, the laser diode with two coupled fibers is the best choice (9% efficient with delivery of 59 mW optical power to the photovoltaic). High efficiency with the lamps or IRED can only be obtained using fiber bundles. Efficiency increases as the number of fibers increases to fill the beam area. When this occurs, the IRED system shows 5% to 7% efficiency for useful optical power generation and delivery to the photovoltaic. The corresponding efficiencies for the arc and W-X_2 lamps are 2% to 5% and 3% to 6%, respectively. The largest amount of optical power carried in a fiber (210 mW (-54°C) to 280 mW (260°C)) occurs with the 300W arc lamp and the 1000-μm-core fiber. A bundle of fifty-five such fibers could carry over 10 Watts of usable optical power from a single 300W arc source. Unless lenses are used at the photovoltaic, the photovoltaic area would have to be at least as large as the beam area for both the lamps and IRED in order to utilize all the optical power carried by the fiber optic bundle.

Source comparisons, previously mentioned, are summarized in Items IV.C to IV.E. The efficiency factor for thermoelectric cooling of the IRED is higher than for the ILD because only two cooling stages are required. This IRED can operate with long life up to about 65°C ambient compared to 35°C for the ILD. Although the lamps are high-temperature sources, their continued operation demands that heat be constantly removed. Since the lamps must be operated continuously, there is a high duty-factor penalty associated with pulse-width modulation of the photovoltaic output. Lifetime is longest for the solid-state sources. The lifetime of any of the sources can be increased by reducing their input electrical power.

Further discussion on choice of optical source will be made after a discussion of photovoltaic design and power-conversion efficiency.

TABLE XV

ESTIMATED POWER-BY-LIGHT EFFICIENCIES

Category	ILD$_o$ 8200Å 0.64W	IRED$_o$ 8200Å 0.35W	Xe Arc Lamp Short Arc 300W	Xe Arc Lamp Short Arc 150W	W-X_2 Lamp (3200°K) 13W	W-X_2 Lamp (3200°K) 250W
I. Optical Power Generation and Delivery to GaAs Photovoltaic						
A. Source E→O (Useful for PV)						
$\lambda \leq 8250$Å:	18.8%	15.7%	18.5%	18.5%	19.5%	19.5%
$\lambda \leq 8700$Å:			21.3%	21.3%	22.5%	22.5%
$\lambda \leq 9130$Å:			24.0%	24.0%	25.5%	25.5%
B. Optical Coupling to Fiber(s)						
1. Efficiency						
(a) d_c=200μm(NA=0.55)	80%	52%	24%	20%	26%	26%
(b) d_c=1000μm(NA=0.3)	60%	63%	30%	25%	33%	33%
2. No. of fibers in array						
(a) d_c=200μm(NA=0.55)	2	17	302	210	215	3292
(b) d_c=1000μm(NA=0.3)	2	3	55	39	39	606
3. Beam area (cm^2)						
(a) d_c=200μm(NA=0.55)	2×10^{-4}	0.009	0.16	0.11	0.12	1.8
(b) d_c=1000μm(NA=0.3)	10^{-3}	0.033	0.59	0.42	0.43	6.5
C. Fiber Transmission-10 meters						
(a) d_c=200μm(NA=0.55)	97%	97%	76-81%	77-82%	90-92%	90-92%
(b) d_c=1000μm(NA=0.3)	99%	99%	95-96%	95-96%	98%	98%
D. Two-Connector Transmission						
(a) d_c=200μm(NA=0.55)	63%	63%	63%	63%	63%	63%
(b) dc=1000μm(NA=0.3)	75%	75%	75%	75%	75%	75%
E. Totals for Optical Power Generation and Delivery to PV						
1. Efficiency						
(a) d_c=200μm (NA=0.55) $\lambda \leq 8250$Å:	9.3%	5.0%	2.1%	1.8%	2.9%	2.9%
$\lambda \leq 8700$Å:			2.5%	2.1%	3.3%	3.3%
$\lambda \leq 9130$Å:			2.9%	2.4%	3.8%	3.8%
(b) d_c=1000μm (NA-0.3) $\lambda \leq 8250$Å:	8.5%	7.4%	3.9%	3.3%	4.7%	4.7%
$\lambda \leq 8700$Å:			4.5%	3.8%	5.4%	5.4%
$\lambda \leq 9130$Å			5.1%	4.3%	6.2%	6.2%
2. Optical Power in fiber array (Watts)						
(a) d_c=200μm (NA=0.55) $\lambda \leq 8250$Å:	0.059	0.018	6.2	2.7	0.37	7.2
$\lambda \leq 8700$Å:			7.4	3.2	0.44	8.4
$\lambda \leq 9130$Å:			8.6	3.6	0.50	9.6
(b) d_c=1000μm (NA=0.3) $\lambda \leq 8250$Å:	0.052	0.026	11.7	4.9	0.61	11.8
$\lambda \leq 8700$Å:			13.6	5.7	0.71	13.6
$\lambda \leq 9130$Å:			15.3	6.4	0.80	15.4

TABLE XV (Cont'd)

ESTIMATED POWER-BY-LIGHT EFFICIENCIES

Category		ILD 8200Å 0.64W	IRED 8200Å 0.35W	Xe Arc Lamp Short Arc 300W	Xe Arc Lamp Short Arc 150W	$W-X_2$ Lamp (3200°K) 13W	$W-X_2$ Lamp (3200°K) 250W
II. Maximum Photovoltaic O → E Efficiency for wavelengths shorter than the absorption edge of GaAs							
	-55°C:	49%	49%	38-36%	38-36%	41-40%	41-40%
	25°C:	43%	43%	34-32%	34-32%	36%	36%
	260°C:	21%	21%	18-17%	18-17%	18%	18%
III. Maximum Overall System Efficiency (E→E) *							
(a) d_c=200μm (NA =0.55)	-55°C:	4.6%	2.5%	0.79%	0.67%	1.17%	1.17%
	25°C:	3.9%	2.1%	0.86%	0.72%	1.22%	1.22%
	260°C:	2.0%	1.05%	0.51%	0.43%	0.71%	0.71%
(b) d_c=1000μm (NA=0.3)	-55°C:	4.1%	3.6%	1.39%	1.17%	1.88%	1.88%
	25°C:	3.6%	3.1%	1.46%	1.23%	1.94%	1.94%
	260°C:	1.8%	1.55%	0.86%	0.72%	1.12%	1.12%
IV. Miscellaneous Comparisons							
A. PV Electrical Power Per Fiber (PV Impedance Matched to load) (mW/fiber)							
(a) d_c=200μm (NA=0.55)	-55°C:	15	0.55	7.8	4.8	0.71	0.89
	25°C:	13	0.44	8.5	5.2	0.73	0.92
	260°C:	6	0.22	5.1	3.1	0.43	0.54
(b) d_c=1000μm (NA=0.3)	-55°C:	13	4.2	76	45	6.3	7.8
	25°C:	12	3.7	80	47	6.5	8.0
	260°C:	6	1.8	47	28	3.7	4.6
B. PV Electrical Power Per Area of glass at 25°C (PV Impedance Matched to load) (W/cm^2)							
(a) d_t=250μm (NA=0.55)		26	0.89	17.3	10.5	1.50	1.88
(b) d_t=1111μm(NA=0.3)		1.2	0.38	8.2	4.9	0.67	0.83
C. Source Cooling Efficiency from Possible 125°C ambient		12%	25%	Forced fluid cooling is required			
D. Duty-Factor Efficiency		100%	100%	5-50%	5-50%	5-50%	5-50%
E. Estimated Source Lifetime (Hours)		$>10^4$	$>10^5$	300	300	75	100

*(1) Power supply efficiency and source cooling are not taken into account
(2) Assumes no Duty-Factor Penalty for Lamps
(3) Assumes loss-less photovoltaic impedance matching to load

9.2 Photovoltaic Design

The choice of GaAs as the photovoltaic material in a power-by-light application was based on (1) the availability of high-power solid-state injection laser diodes which emit at a wavelength just above the GaAs band-gap energy and can be readily coupled to a single optical fiber, (2) the value of the GaAs energy gap in relation to the temperature range of performance and (3) the relatively high GaAs technology level which permits construction of photovoltaic solar cells that exhibit high power-conversion efficiency (20-24% near room-temperature). The essential operating difference between the power-by-light photovoltaic and the solar cell is the spectrum of the incident light, which can be nearly monochromatic (solid-state sources) or have some distribution (lamps). As a result, GaAs solar-cell design, construction and performance can be used as a starting point for specifying a power-by-light photovoltaic and for estimating photovoltaic power-conversion efficiency.

During solar-cell operation, incident photon energies less than the energy gap of the absorbing medium cannot contribute to cell output by way of electron-hole generation. Photon energies in excess of the band-gap energy can create the necessary electron-hole pairs but the excess energy will excite lattice vibrations (converted to heat). For a GaAs solar cell only about 40% of the sun's energy can be used in electron-hole generation (Ref. 19). In the power-by-light photovoltaic, the wavelength of a solid-state source can be matched to the GaAs band gap so that not only are all the photons usable but the energy in excess of the energy gap can be minimized. As a result, overall power-conversion efficiency will be higher compared to a solar flux. The cell will operate cooler and have lower series resistance for a given photon flux or be able to operate at a higher incident flux and electrical output at a given temperature. As will be discussed later, beneficial changes can be made in GaAs solar-cell designs to take advantage of a nearly monochromatic source. In the case of the lamps, the spectral output will be changed by the absorption characteristics of the optical fiber. The cutoff for usable energy is the absorption edge of the GaAs.

In solar-cell fabrication, one goal is to make as large an active semiconductor area as possible (e.g., square inches) to reduce the number of cells in large-scale terrestrial or space applications. In the power-by-light application, the optical energy could be coupled and transmitted on the aircraft using a single fiber, e.g., a core diameter of 200 μm. Physically, the photovoltaic area would then be orders of magnitude smaller than the solar cell, and the sealed package could be constructed with an integral fiber-optic pigtail for activation with the fiber tip placed closed to the photovoltaic cell. If 30 mW of optical power emanated from the fiber, then optical power densities considerably in excess of that due to the solar flux would be incident on the photovoltaic cell. For a photovoltaic with a diameter of

300 μm, there would be incident 42 watts/cm^2 which corresponds to 420 AM1 suns. If a fiber bundle were used to transmit the power, then a photovoltaic area larger than the focussed beam area (Item B.3 in Table XV) could be used. If 12 watts from an arc lamp were carried in a bundle to a cell with 0.25 cm^2 area, 48 watts/cm^2 would be incident on the photovoltaic. The use of a lower-brightness tungsten-halogen lamp would require a much larger photovoltaic area for the same optical power. The actual photovoltaic area and array distribution will be determined by cell current-voltage characteristics, cell internal series resistance, type of source and impedance matching to a given load. In any case, solar cell designs suitable for concentrator systems are particularly suitable for power-by-light photovoltaic designs.

One factor that will ultimately limit the optical concentration that can be used is the internal series resistance of the cell. High internal resistance reduces the maximum-power output (or fill factor) of the cell. The fill factor (FF) is an important measure of cell performance and is defined as:

$$FF = \frac{V_{mp}\, J_{mp}}{V_{oc}\, J_{sc}} \qquad (9\text{-}1)$$

Here, V_{mp} and J_{mp} are the voltage and the current density at the maximum-power point, V_{oc} is the open-circuit voltage and J_{sc} is the short-circuit current density. As series resistance increases in a cell, both J_{sc} and FF are reduced. The most important effect is in reduction of FF through lowered V_{mp} and J_{mp}. Two important factors in concentrator design are minimization of (1) sheet resistivity of the surface layer on which the finger pattern is placed and (2) contact resistance of metallization to the semiconductor surface. Proper cell design is the result of balances between many conflicting trends. For example, there is a balance between close finger spacing on the top surface of the device for reduced resistance and loss of optical real estate by placing more metallization on the surface. Another trade-off is that as top layer thickness is increased, the sheet resistivity decreases but there is an increase in optical absorption before reaching the GaAs p-n junction. Shunt resistance is a minor factor compared to series resistance and will not be discussed further.

Various GaAs solar-cell designs have been reported in the literature. The two types that are most appropriate for stable high-temperature concentrator application are the GaAlAs heterostructure (heteroface) and GaAs homojunction cells. Less is known about the performance of GaAs Schottky Barrier or Metal-Insulator-Semiconductor cells especially at high temperature. These are not being considered for this program due to uncertainties in the stability of the GaAs surface. Polycrystalline cells are not suitable due to lower overall cell efficiency. Cascade cells are not required for a nearly monochromatic source, but could be used to boost photovoltaic power-conversion efficiency for lamp sources. Cascade cells are constructed of two or more monolithic heteroface cells and were not considered in this study.

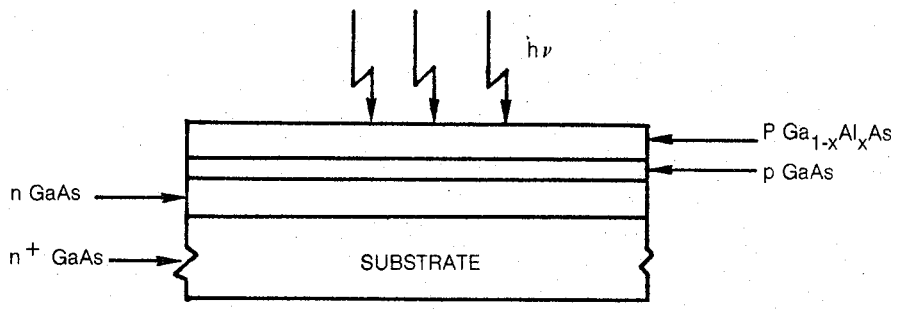
Cross-sectional schematics of heteroface and homojunction solar-cell structures are shown in Fig. 9-1. In either case, a GaAs p-n junction provides the built-in potential barrier for collection of the generated electron-hole pairs. Absorption is direct in GaAs so that only a few microns of GaAs are required. The heteroface cell utilizes a $Ga_{1-x}Al_xAs$ layer to act as a transparent window for absorption in the underlying GaAs and to confine minority carriers below the interface. This will reduce surface recombination velocity and increase cell efficiency.. Due to the excellent lattice match between GaAs and AlAs, the recombination velocity is over 100-times smaller at the heterojunction compared to a GaAs surface (Ref. 20) and is therefore beneficial for increased efficiency. For solar application, the aluminum content, x, is greater than 0.8 in order to extend transparency to as short a wavelength as possible. Only two layers are grown on the p^+ substrate; the p-GaAs layer is formed by intentional diffusion of the p dopant out of the ternary layer. The complimentary growth heterostructure ($N/p/p^+$) is actually a heterojunction cell due to lack of n-type diffusion and has not yielded as high a power-conversion efficiency as the $P/p/n/n^+$ structure. Several concentrator designs incorporating variations in thickness of the layers, aluminum atom fraction, carrier concentrations, grid pattern, and alloy contact have been reported (see for example, Refs. 21 to 25).

In the GaAs homojunction structure shown in Fig. 9-1b (Ref. 26), the p-n junction is located within about 600Å of the surface. Although some absorption takes place in the n^+ layer and significant hole recombination may occur at the nearby GaAs surface as a result, most of the carriers are generated in the p-layer and can be usefully collected. The sheet resistivity of the thin n^+ layer is comparable to the thicker p-type ternary layer of the heteroface cell in Fig. 9-1a.

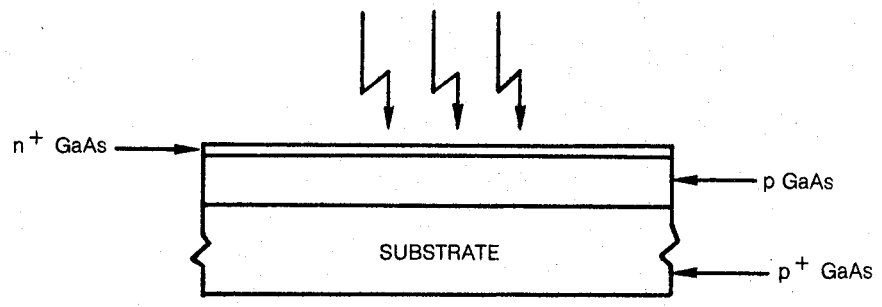
FIG. 9-1

SOLAR-CELL STRUCTURES FOR POWER-BY-LIGHT PHOTOVOLTAIC APPLICATION

a) HETEROFACE ($P/p/n/n^+$):



b) HOMOJUNCTION ($n^+/p/p^+$):



82-8-34-2

Table XVI contains a listing of power-conversion efficiency for various concentrator solar-cell designs. Overall cell efficiency can be 20% even at a solar concentration of 1000. In general, efficiency should increase gradually with solar concentration and peak as cell internal series resistance becomes an important factor. The lower the value of series resistance then the greater is the cell efficiency at high solar concentration. Excess temperature rise caused by the concentrated sunlight will further increase resistance and reduce cell efficiency. A broad peak between 30 and 150 AMO suns is expected for the heteroface cells with moderate heat sinking (Ref. 27). In Table XVI one cell exhibited a peak in efficiency at 178 AM1 suns (Ref. 23). The high resistance for the homojunction structure was due to a high contact resistance. A possible fabrication problem here is forming a good alloyed contact to a 1000Å n^+-GaAs layer without disturbing the p-n junction. Another negative factor is the critical nature of the n^+ thinness in the active region. Based on the cell efficiencies in Table XVI, it appears that the heteroface GaAs structure is a better choice for a high-efficiency power-by-light cell.

A summary of performance data collected from the literature on open-circuit voltage, short-circuit current density and fill factor for heteroface GaAlAs/GaAs solar cells as a function of temperature is shown in Figs. 9-2 and 9-3. Similar temperature dependences are expected for the power-by-light photovoltaic. These data will be used in discussions on power-by-light (1) photovoltaic impedance matching to the torque-motor load, (2) photovoltaic array size, and (3) photovoltaic device size.

Figure 9-2 primarily shows open-circuit voltage data for a variety of exposure conditions. Shown are two cases (Refs. 2 and 28) for data over a wide temperature range as well as more limited temperature ranges and fixed points for representative cells near room temperature. Here the notation, mX, refers to m times the solar flux for the particular air-mass (AM) condition. AM does not have much effect on cell voltage; however, as solar concentration increases from 1X, V_{oc} and V_{mp} will increase, eventually level off, and finally decrease. V_{oc} decreases at high concentration due to heating and V_{mp}, fill factor and cell efficiency decrease as cell series resistance increases. For power-by-light application, operation is therefore indicated at as high an incident optical flux as possible but consistent with internal cell resistance and impedance matching to the load. The temperature coefficient of V_{oc} under concentration favors the data from Ref. 2. This temperature dependence was, therefore, used to predict power-by-light photovoltaic high-temperature performance. The absolute value of V_{oc} and V_{mp} from Ref. 2 are also reasonable starting points for analysis, but these values could be up to 20% higher under proper optical concentration.

TABLE XVI

CONCENTRATOR SOLAR-CELL EFFICIENCIES

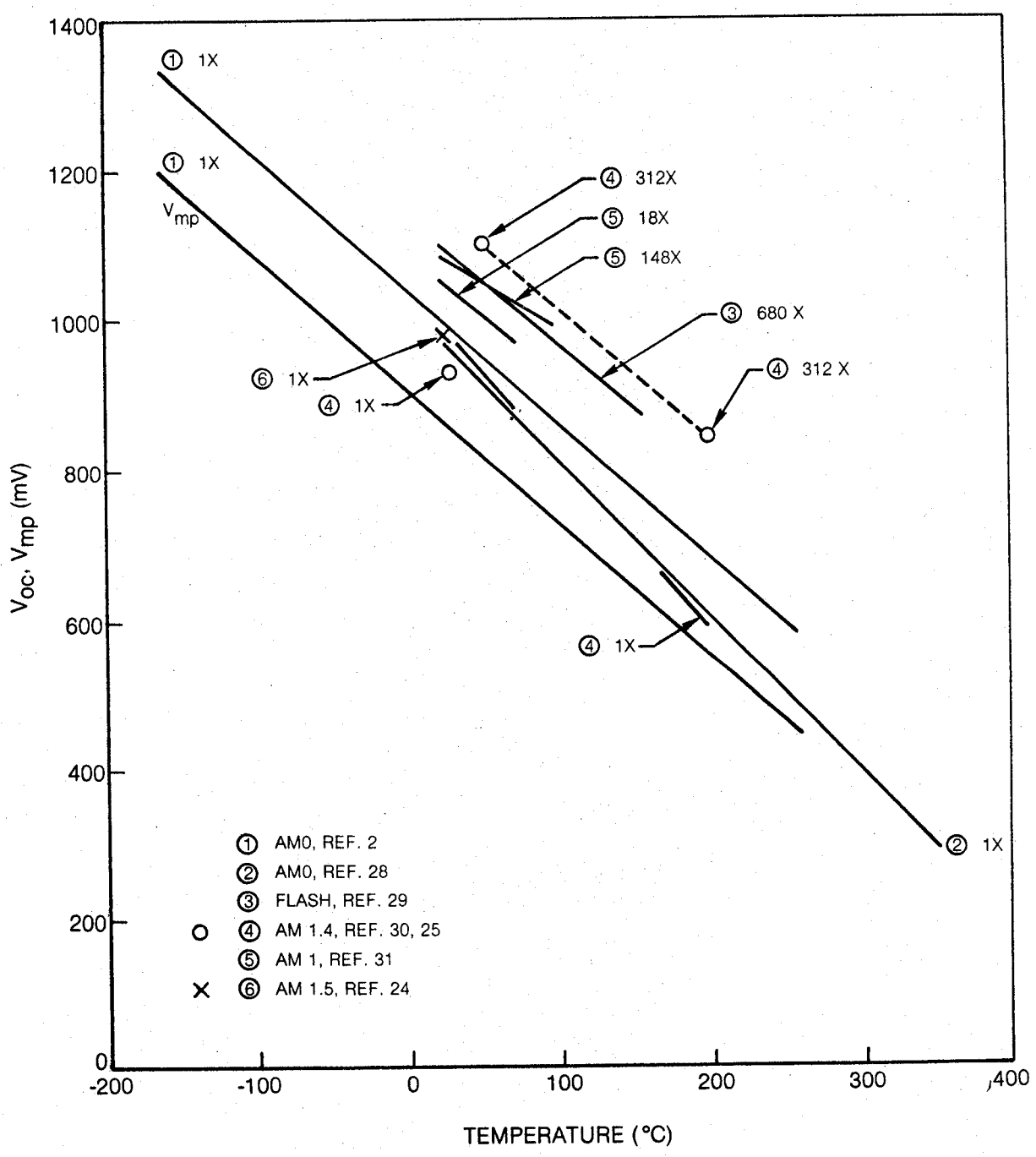
Cell Type** And Area	Power-Conversion Efficiency	Output Power (W/cm^2)	Solar Concentration (# of Suns)	Air Mass	T (°C)	R_S (ohm-cm^2)	Reference
Heteroface ($Ppnn^+$) 1 cm^2	22.3%	--	197	1	*	0.01	21
	21.8%	--	326				
	21.3%	--	500				
	20.0%	20	1006				
Heteroface (p^+Ppnn^+) 0.57 cm^2	23.3%	19	945	1.5	*	--	22
Heteroface (Ppn) 0.79 cm^2	24%	--	74	1	50	0.02	23
	24.7%	--	178				
	21.2%	--	270				
	20.3%	--	440				
	22.5%	--	365	2	65	0.0005	23b
	22.3%	--	596				
	21.7%	--	899				
Heteroface (Ppn) 0.132 cm^2	17%	--	30	1.5	<100	0.04	24
	16%	--	100				
	11%	6	600				
Heteroface ($Ppnn^+$)$_2$ 1.26 cm^2	22%	0.8	43	1.4	51	0.027	25
	17.5%	4.5	312		54		
	14%	3.45	312		200		
Homojunction (n^+pp^+) 0.47 cm^2	22%	--	19	1	*	> 0.1	26
	17%	--	325				

* Assume near-room temperature ambient and heat sinking or pulse measurements.

** Upper case letter for $Ga_{1-x}Al_xAs$

FIG. 9-2

VOLTAGE DATA FOR GaAs HETEROFACE SOLAR CELLS



82-10-9-6

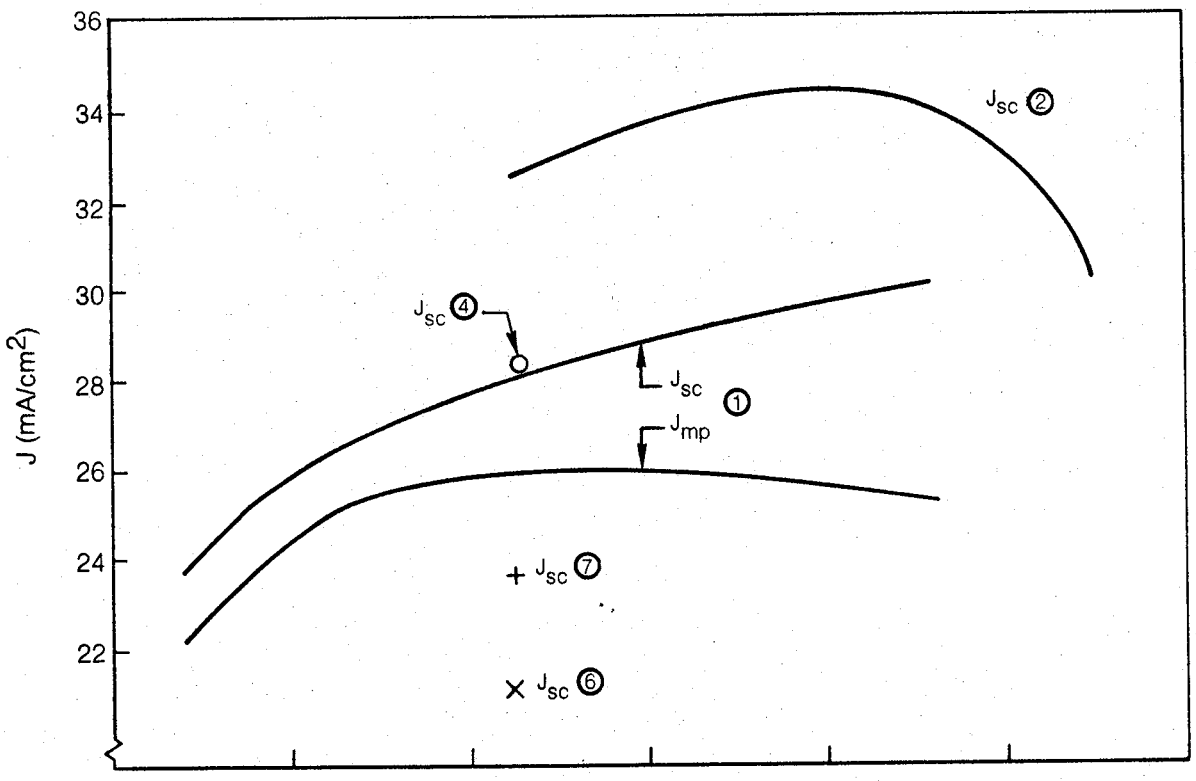
Short-circuit current density and maximum-power current density are shown in Fig. 9-3a and FF in Fig. 9-3b. Good fill factors range from 0.8 to 0.86 for GaAs heteroface cells near room temperature. The lower FF for the Ref. 28 data may be due to a higher cell series resistance compared to the other cells. Some extra data points are shown in Fig. 9-3b for the case of very-high-efficiency concentrator solar cells. High FF and cell efficiency can be maintained at high concentration only if cell series resistance is very low (in this case, R_S = 0.005 ohm-cm^2). Cell current density depends not only on incident optical concentration but on the particular AM condition. The current density level will also vary depending on the percentage of the active area obscured by an ohmic-contact grid. Note that for a given solar flux, J_{sc} has little temperature dependence. A slight increase with temperature occurs due to an increase in minority carrier diffusion lengths and perhaps energy-gap narrowing. Eventually, cell series resistance will be high enough to limit output current.

The power-by-light photovoltaic must have high efficiency and function at up to 260°C. GaAs heteroface solar cells have demonstrated high conversion efficiency up to 1000 suns, and one has been operated at 14% power-conversion efficiency at over 300 suns at 200°C (Ref. 25 in Table XVI). Since GaAs band-gap energy increases as temperature decreases, the highest useful wavelength for a solid-state source must be based on the energy gap at the lowest application temperature, -54°C. Based on GaAs energy-gap data as a function of temperature (Ref. 1) and solar-cell response data at room temperature (Ref. 23b), about 90% internal collection will commence at about 8250Å at -54°C. An 8200Å emitter is therefore appropriate. The cut-off wavelength of the photovoltaic will increase as temperature increases, and a greater percentage of the total optical energy output of the lamp will be utilized at the photovoltaic. As a result, the lamp could be said to show improved electrical-to-optical power-conversion efficiency. Due to lamp spectral output in the visible, the power-by-light heteroface photovoltaic will be very similar in epitaxial-layer characteristics to the heteroface solar cell.

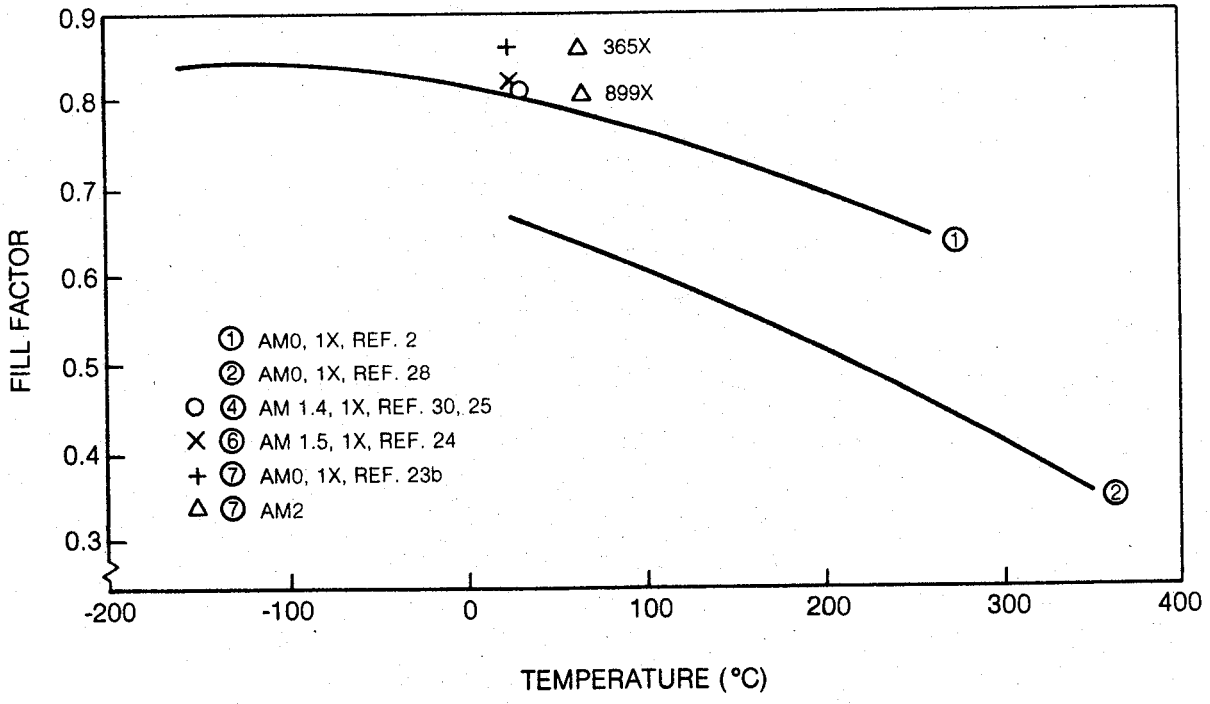
When using a solid-state source, beneficial changes can be made in the design of the heteroface cell. If the source wavelength is 8200Å, the $Ga_{1-x}Al_xAs$ window layer need only contain sufficient aluminum to place its energy band gap higher than 1.51 eV at 260°C. Using $Ga_{1-x}Al_xAs$ band-gap data (Ref. 32) and assuming a band-gap dependence on temperature similar to that for GaAs, then x should be greater than 0.16. This is substantially less than the best solar cells where x is near 0.9. As x increases, the resistivity of both N- and P-type $Ga_{1-x}Al_xAs$ increases for constant carrier concentration. The effect is quite dramatic for N-type near x = 0.4 and more continually varying for P-type (Refs. 24 and 33). A closely related problem is that as x increases, it becomes incresingly more difficult to make ohmic contact to the ternary layer, presumably due to oxide intermediates. The high resistivity of thin $Ga_{1-x}Al_xAs$ layers and contact difficulty have led to some

GaAs HETEROFACE SOLAR-CELL CHARACTERISTICS

a) CURRENT DENSITY AT ONE-SUN ILLUMINATION



b) FILL FACTOR



82-10-9-4

solar-concentrator designs where contact is made by using a p^+-GaAs layer under the grid (Ref. 22). Alternatively, contact may be made directly to a thicker p-GaAs layer through an etched-out grid pattern in the ternary layer (Refs. 23 and 24). The series resistance problem becomes more serious in some concentrator designs where the thickness of the $Ga_{1-x}Al_xAs$ is minimized (especially in space application) so that a larger fraction of solar photons with energy greater than the $Ga_{1-x}Al_xAs$ bandgap can be utilized and radiation damage effects can be reduced. In the power-by-light cell, the contact problem will be reduced when using solid-state sources because of reduced aluminum content. The sheet resistivity will also be lower for the same reason and because the thickness of transparent $Ga_{1-x}Al_xAs$ can be increased. It may then be possible to increase the separation between fingers of the contact grid to expose more photosensitive area. Furthermore, only a single anti-reflection coating would be necessary for the power-by-light cell. Other factors, such as layer carrier concentration and thickness of p- and n-GaAs layers would remain the same as for the solar cell. In summary, due to the nearly monochromatic source, some changes can be made in typical heteroface solar-cell design to result in reduced series resistance and greater ease of fabrication. The lower resistance improves cell efficiency under optical concentration.

Photovoltaic size in a power-by-light application is strongly influenced by the internal series resistance of the cell. Cell operation under concentrated light could give up to 20% higher power-conversion efficiency. To take advantage of concentration, the fiber(s) should be placed as close as possible to the photovoltaic active area which in turn should be larger than the fiber area in order to capture most of the light leaving the end of the fiber (NA effect). The optical density on the power-by-light cell will have to be such that the internal series resistance (R_S) is small compared to the ratio, V_{oc}/J_{sc}, in order to preserve cell fill factor and calculated output efficiency. The inequality has to be satisfied at the highest application temperature since V_{oc} is at its lowest and R_S is at its highest values. Extrapolation of the series-resistance data for the heteroface GaAs cell of Ref. 29 to 260°C shows that the cell series resistance will be almost 50% higher than at room temperature. The best concentrator cells have R_S of 0.005 to 0.01 ohm-cm^2 at room temperature (Ref. 23b and 21). More often, observed values are 0.02 to 0.04 ohm-cm^2 (Refs. 23b, 24, and 40). With 21.5 mW incident on a cell at 260°C with an R_S of 0.06 ohm-cm^2, R_S will be approximately equal to V_{oc}/J_{sc} for a cell diameter of 0.04 cm. Cell diameter has to be appreciably larger than this value to maintain fill factor and power-by-light power-conversion efficiency.

In order to estimate the effect of internal series resistance on the power-by-light efficiency of the photovoltaic cells, use has been made of the formulation by Green (Ref. 34). In this method, the effect of cell series resistance, temperature and diode ideality factor on cell fill factor can be calculated for any cell given values of V_{oc} and J_{sc}. An important parameter is the cell resistance factor, r_f defined as

$$r_f = \frac{R_S J_{sc}}{V_{oc}} = \frac{R_S I_{sc}}{a_p V_{oc}} \qquad (9\text{-}2)$$

where a_p is the cell area. In Green's treatment the relatively small effect of R_S on J_{sc} for values of r_f up to 0.4 were neglected. The diode ideality factor, n_f, is not often cited with published solar-cell data. One reference that does supply this value for a cell having fill factor and open-circuit voltage near the Ref. 2 room-temperature data is Ref. 24. These data were included as singular points in Figs. 9-2 and 9-3. The cited diode factor was 1.67 and R_S was 0.041 ohm-cm^2. The calculated fill factor using Green's method for the Ref. 24 data agrees with the measured value of 0.82 at room temperature. If the n_f value is representative of the Ref. 2 cell, then calculations can be made to establish the effect of R_S on cell performance at high temperature. For these calculations it was assumed that the diode ideality factor did not change with temperature; some support for this assumption is given in Ref. 28. Figure 9-4 shows plots of the resistance factor versus fill factor for two temperatures. The theoretical limits for zero series resistance are shown for each curve. Extra abscissa scales show the fractional power (fill factor) decrease as r_f increases. If the photovoltaic cell is impedance matched to the torque-motor coils at 260°C and if an arbitrary maximum loss in fill factor is accepted, then a maximum r_f can be picked from Fig. 9-4. Using Eq. (9-2), curves of R_S versus cell diameter can be plotted. Curves for specific conditions on number of fibers per cell and maximum acceptable power-conversion-efficiency loss (ΔPCE) are shown in Fig. 9-5. For this example, each fiber was carrying 21.5 mW (λ=8200Å). If a maximum 5% loss in fill factor is set at 260°C for the one-fiber case, then photocell diameter would have to be at least 2 mm for a cell R_S of 0.06 ohm-cm^2. This corresponds to 0.68 W/cm^2 or the optical energy equivalent of 6.8 AM1 suns. If a 9% loss figure is acceptable, then the same minimum diameter would be required for 2 fibers per cell (1.4 W/cm^2 or 14 AM1 suns). It is important to note that the cell area must scale with illumination intensity to maintain a selected fill-factor tradeoff. At the above incident light levels, about 3-5% increase in open-circuit voltage would be expected over the one-sun AM1 condition; this would partially offset the 5-9% loss in fill factor due to R_S. At lower temperatures, the r_f factor is less and loss will be a lower percentage. Similar calculations can be made for larger fiber bundles as in the case of lamp sources.

EFFECT OF SERIES RESISTANCE ON CELL FILL FACTOR

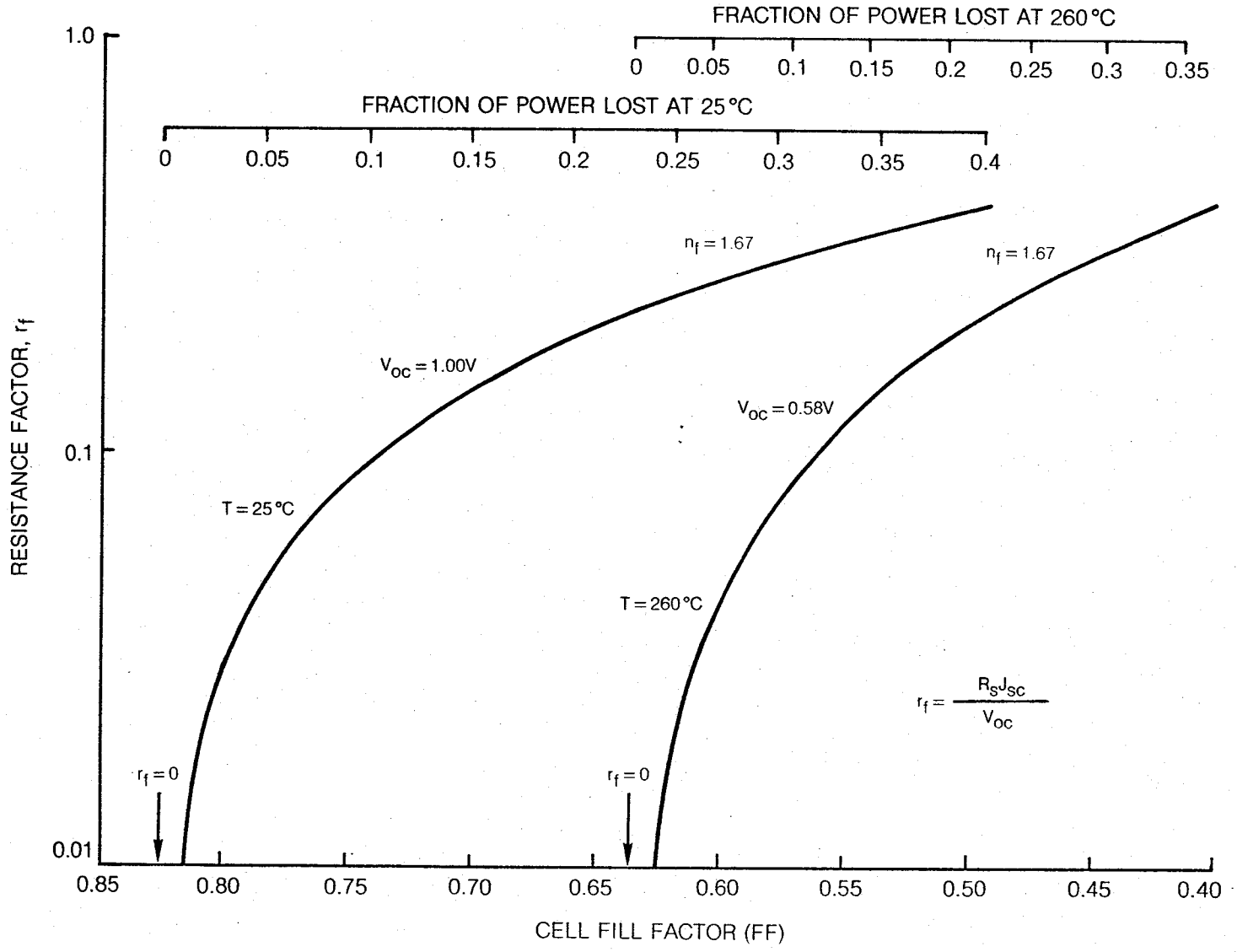
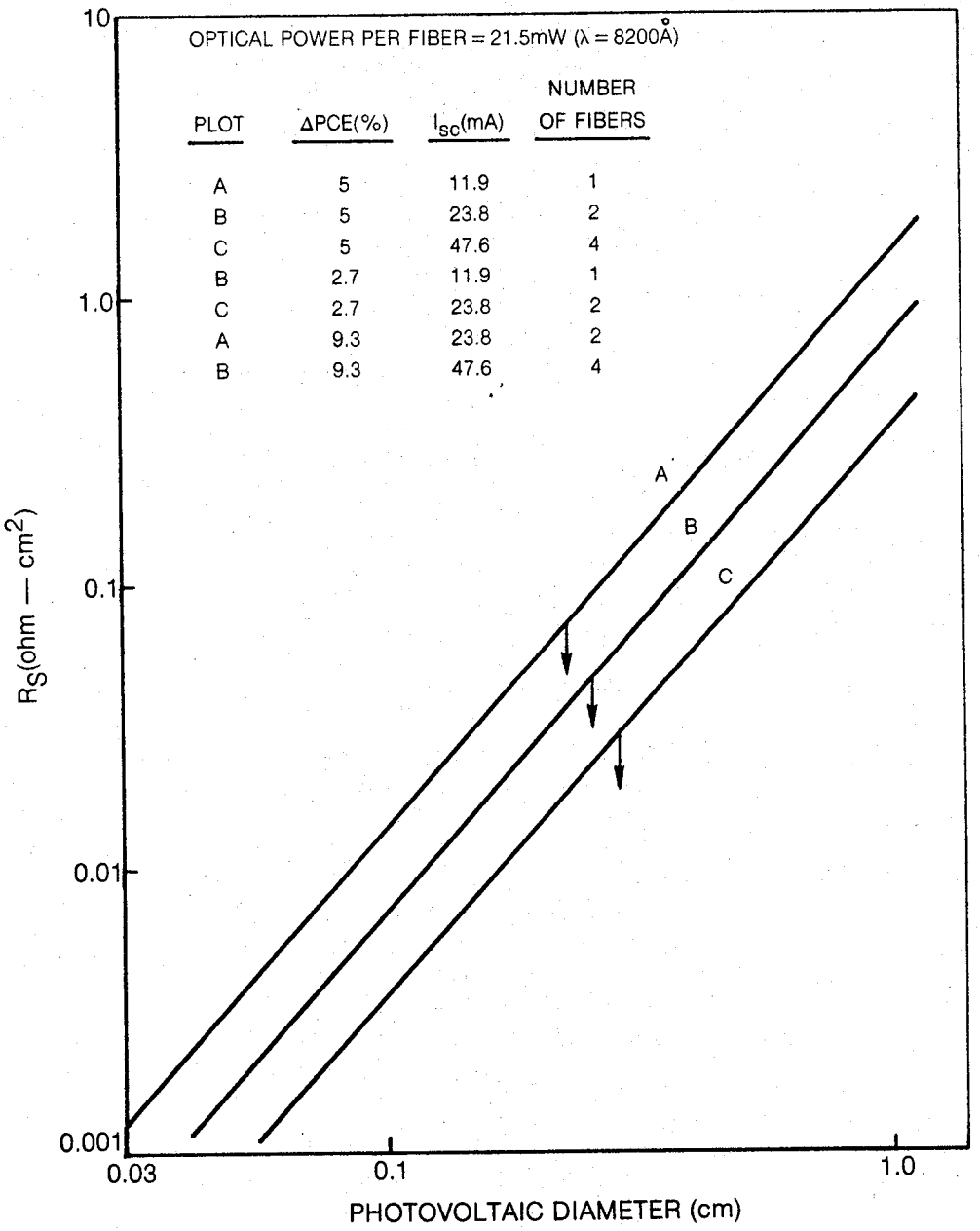


FIG. 9-4

FIG. 9-5

MAXIMUM PHOTOVOLTAIC SERIES RESISTANCE VS DIAMETER FOR VARIOUS OPERATIONAL CONDITIONS

$T = 260°C$
$V_{oc} = 0.58V$
$n_f = 1.67$



82-10-9-7

In the hardware phase of the program good butt coupling results were obtained with the 200 μm-core fiber and 200-μm-diameter phototransistor. Coupling of single fibers with 1-to-2-mm-diameter photovoltaic cells requires that fiber(s) must be placed far enough from the cell (related to fiber NA) so as to maintain a specified optical concentration - fill factor balance. With larger separation, coupling of multiple fibers is more easily accomplished. Optical power emanating from a fiber end will have a Gaussian distribution. In general, a distribution of light intensity will exist within a photovoltaic bundle and across the photovoltaic. Non-uniform light intensity will also lead to lower cell efficiency compared to the uniform case.

9.3 Power-by-Light Photovoltaic and System Efficiency

According to Table XVI, solar power-conversion efficiencies in excess of 20% are achievable at high solar concentration near room temperature. Using solid-state sources the power-by-light cells will have higher efficiency due to the monochromatic wavelength which is matched to the semiconductor band gap. An estimate of photocell power-conversion efficiency (η) can be made using Eq. (9-3) (Ref. 35). Here, η is the ratio of the electrical power output to the optical power arriving per unit area.

$$\eta = Q(1-r)(1-e^{-\alpha\ell}) \frac{\Lambda V_{mp}}{1 + \Lambda V_{mp}} \frac{q\, n_{ph}(E_g) V_{mp}}{N_{ph}\, E_{av}} \qquad (9\text{-}3)$$

Q	Fraction of generated carriers that are collected.
$(1-r)$	Surface transmission coefficient (use anti-reflection coating).
$(1-e^{-\alpha\ell})$	Fraction of radiation absorbed
Λ	$\sim q/kT$
V_{mp}	Voltage delivered at maximum power
q	Electronic charge
$n_{ph}(E_g)$	Number of photons/sec/area of p-n junction with sufficient energy to generate electron-hole pairs.
N_{ph}	Total number of incident photons
E_{av}	Average energy of incident photons

The best available literature data for V_{mp} as a function of temperature for a heteroface cell were shown in Fig. 9-2. The cell output voltage versus temperature is principally influenced by changes in the cell dark-current density, which depends on material parameters such as energy gap, doping densities, minority-carrier lifetimes, diffusion coefficients, and carrier recombination. Voltage output will be affected by cell series resistance and concentration level. Reasonable values for the various factors in Eq. 9-1 are given in Table XVII with V_{mp} obtained from Fig. 9-2. Since all the incident photons can produce electron-hole pairs, then $n_{ph}(E_g) = N_{ph}$. An extra factor (0.90) was used to take account of photons blocked by a required top-surface opaque metallization grid. The expected photovoltaic power-conversion efficiencies for quality cells at the maximum-power points using the monochromatic sources are 49% (-54°C), 43% (25°C), and 21% (260°C). In actual practice these efficiencies will vary. Operating the photovoltaic under concentrated light will increase efficiency (up to about a factor of 0.2) but all other mechanisms (e.g., carrier recombination, diffusion, series resistance, etc.) will decrease cell efficiency. Operation of the cell off the maximum-power point of the I-V curve will further decrease power-conversion efficiency.

Photovoltaic efficiency for the GaAs heteroface cell has also been calculated using Eq. (9-1) for the arc and 3200°K tungsten-halogen lamp sources. In Eq. (9-1), the average energy of incident photons will be higher than for the solid-state sources. Keeping other factors the same as in Table XVII and estimating the average energy of radiation in 1000Å intervals between the GaAs absorption edge and 3000Å wavelength for each source, photovoltaic efficiencies were calculated at the maximum-power points and the results are shown in Table XV, Category II. Note that any source wavelength not usable by the photovoltaic has been accounted for in Item I.A of this table and therefore, $n_{ph}(E_g) = N_{ph}$. The emission spectrum of the 3200°K tungsten-halogen lamp peaks near 9000Å and is a slightly better match overall to the GaAs photovoltaic then the xenon arc lamp with its strong emission bands in the infrared. A small variation is seen with the lamps due to enhanced shorter-wavelength absorption by the soft-glass fiber. As a result, the incident photon distribution is shifted more towards the infrared for transmission through the soft glass, and the photovoltaic efficiency increases slightly.

The product of values in Categories I and II of Table XV define the Category-III E→E system efficiency (electrical input at the source compared to electrical output at the photovoltaic) subject to some important assumptions listed at the end of the table. Higher system efficiency results if the 1000-μm-diameter fiber is used with the IRED and lamps. When ranked according to efficiency, the order is ILD (best), IRED, W-X_2 and Xe arc. Respective efficiencies at 260°C are 2%, 1.55%, 1.1%, and from 0.7% to 0.86%. An

TABLE XVII

GaAs HETEROFACE PHOTOVOLTAIC POWER-CONVERSION EFFICIENCY AT 8200 Å WAVELENGTH

	Temperature		
	-54°C	25°C	260°C
Q	0.90	0.90	0.90
(1-r)	0.97	0.97	0.97
α (μm^{-1})	1.2	1.3	1.6
ℓ (μm)	3	3	3
$(1-e^{-\alpha \ell})$	0.97	0.98	0.99
V_{mp} (volts)	1.00	0.86	0.45
$\frac{\Lambda\ V_{mp}}{1 + \Lambda\ V_{mp}}$	0.981	0.971	0.907
E_{av} (ev)	1.512	1.512	1.512
$\frac{n_{ph}\ (E_g)}{N_{ph}}$	1	1	1
η	55%	47%	23%
	49%*	43%*	21%*

* If 10% of active area is masked by an opaque metallization grid.

interesting difference between the solid-state sources and the lamps is the efficiency as a function of temperature. The ILD and IRED emission are very nearly matched to the GaAs photovoltaic at -55°C. The degree of matching and maximum-power voltage decrease as temperature increases and GaAs energy band gap decreases. System efficiency should therefore decrease with increasing temperature. As stated earlier, a greater portion of the lamp spectral output is usable as photovoltaic temperature increases. The increase in usable photons offsets the expected decrease in cell efficiency to give a slight increase in system efficiency for the lamps between -55°C and 25°C and a smaller percentage decrease between -55°C and 260°C compared to the solid-state sources.

Category IV of Table XV summarizes other comparisons between the various sources. Item IV.A shows the resultant photovoltaic electrical power caused by optical coupling of one fiber to any of the sources. These numbers were not normalized by the original source power. The ILD value is for the case with no back-facet coating of the ILD. With the high-NA fiber, the ILD produces the highest photovoltaic power per fiber (6 mW at 260°C). If the 1000-μm-diameter fiber is used, the 300-W arc lamp is the best (47 mW at 260°C). The arc lamp also produces over 8-times more photovoltaic power per fiber than a similar-wattage tungsten-halogen lamp. In Item IV.B, the resulting photovoltaic electrical power is normalized with respect to the fiber cross-sectional area. The ILD utilizes the glass most efficiently and would be the system of choice if, for instance, the cost of optical fibers were the most important factor.

The choice of source for a particular power-by-light system is intimately tied to trade-offs involving system efficiency, photovoltaic power level, lifetime, cost and experimental difficulties (e.g., fiber coupling). Although not all the factors are covered, the data in Table XV can be used as a basis for this choice. Some of this data is plotted in a useful way in Figs. 9-6 and 9-7. The vertical coordinate is the E→E system efficiency (Category III) at 260°C using either the 200-μm or 1000-μm-core fiber. The abscissa represents the corresponding electrical power delivered into a load that is properly impedance matched to the GaAs photovoltaic. Each of the source-fiber systems is represented by a locus of points that correspond to the number of fibers and sources used. Photovoltaic load power increases by increasing the number of optical fibers and light sources. When the maximum number of coupled fibers (Item I.B.2 of Table XV) is reached for each source, another source at rated power is added to the system and the system efficiency is halved. The figures conveniently show the number of sources and fibers (ranked according to efficiency) that would be required to produce a given electrical power in the load with the GaAs photovoltaic at 260°C. Barring additional factors it is clear that for below about 200 mW delivered photovoltaic power, the solid-state sources are preferred. The system efficiency is high and a relatively small number of fibers are required. The IRED is

POWER-BY-LIGHT SYSTEM EFFICIENCY* AT 260°C (f)

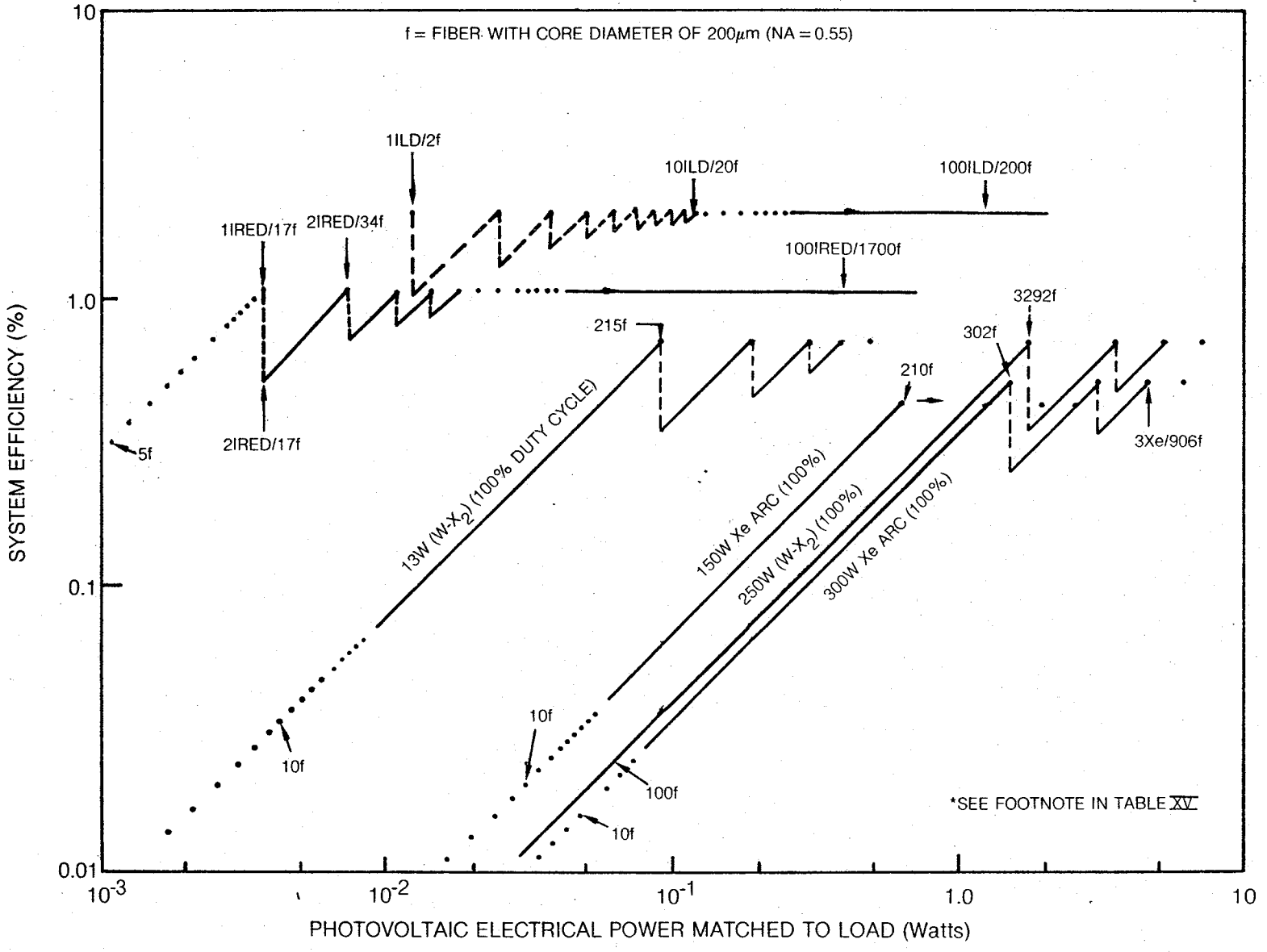
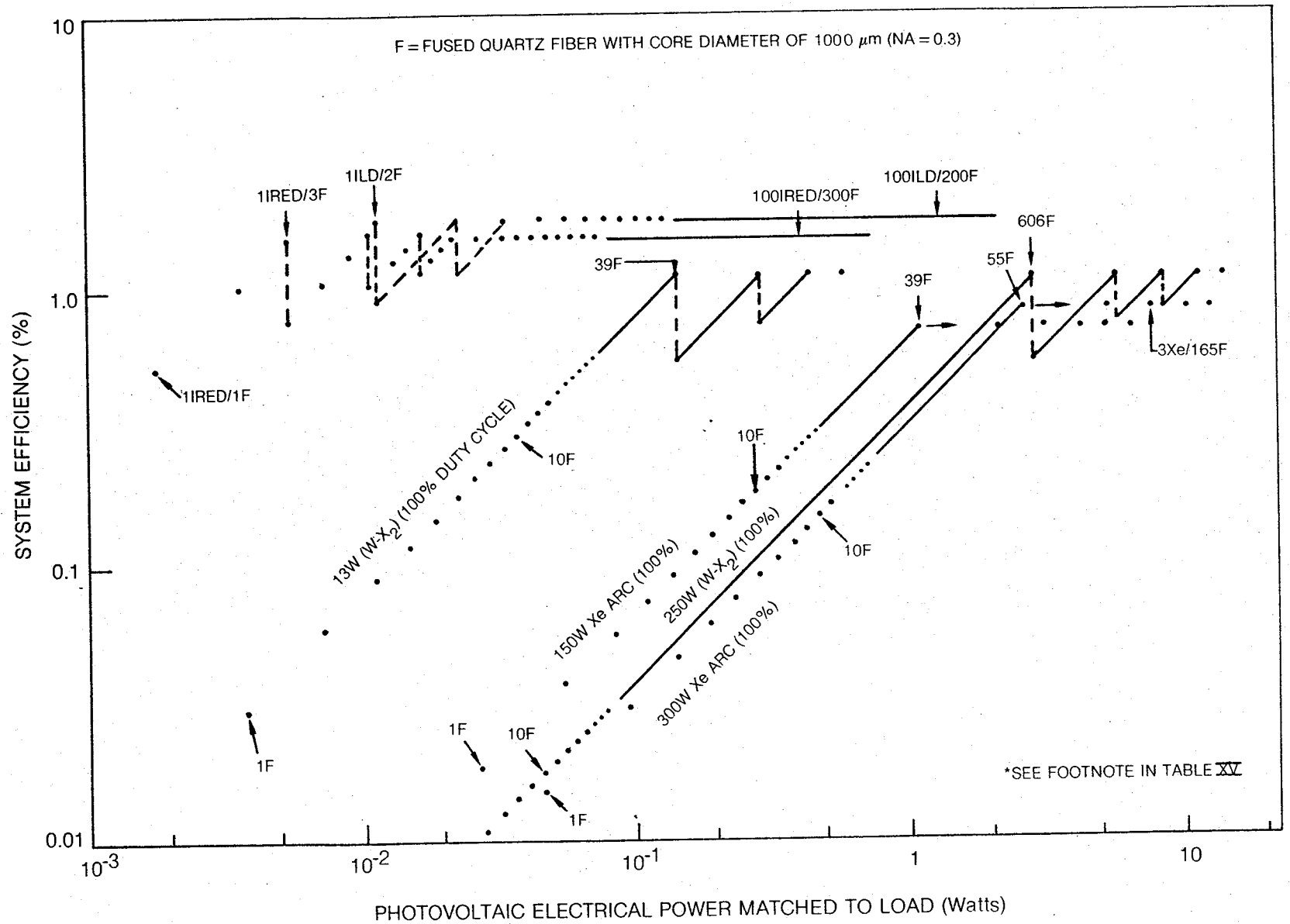


FIG. 9-6

POWER-BY-LIGHT SYSTEM EFFICIENCY* AT 260°C (F)



most competitive with the ILD if the 1000-μm-core fiber is used; however, twice as many sources and three times as many fibers would be required for a given photovoltaic output. For delivered power in excess of 1 watt, the higher-power lamps approach the system efficiency of the solid-state sources at 100% duty cycle. Primary concerns are lifetime differences and costs involved in, for example, providing 100 ILD sources and individual fiber optic lines compared to a single lamp with many coupled fibers. Due to the brightness of the arc lamp, its use would be preferred over a tungsten-halogen lamp to minimize the number of fiber optic lines, but tungsten-halogen lamps are cheaper and easier to operate.

At the photovoltaic there are operational differences that must be noted when using the various sources. Due to the distribution of light in the fiber arrays, each fiber bundle should be associated with one photovoltaic cell. This factor is important when photovoltaic cells are placed in series, since the current output of a series photovoltaic array will be limited by the cell with the lowest output. When using more than one source, balancing of source outputs will be required. This would be done on a per-fiber basis for the ILD and on a per-fiber-array basis for the other sources. Another point is efficient utilization of the photovoltaic surface area. The cross-sectional area of the fiber array is determined by the beam area (Item I.B.3 of Table XV). Barring the use of additional lenses, each GaAs photovoltaic cell would have to be at least as large as the fiber array area. This factor alone would dictate using as high an NA as possible with the lamps, i.e., the 200-μm fiber in these comparisons. The most efficient use of glass and photovoltaic real estate occurs with the laser diode.

On the basis of efficiency and suitability for pulse-width modulation, the laser-diode system is the likely candidate for a demonstration power-by-light system requiring under about 200 mW. In the near future, as technology advances the state of the art, expected optical power output from modulation doped laser diodes should be up to ten-times higher. These devices will not be that much more efficient than present day ILD's but the effect will be to push the ILD curves in Figs. 9-6 and 9-7 to the right and extend the usefulness of laser diode power-by-light systems to photovoltaic outputs of 1 or 2 watts. Above about 2 watts, use of an arc lamp would be more appropriate. Other problem items such as lifetime, source cooling, reduction in efficiency due to duty-cycle penalty, and experimental difficulties associated with, for example, establishing and maintaining a source-fiber lens system and managing fiber arrays, will have to be faced. The effect of increasing the lamp wattage will not necessarily increase efficiency since the beam spot size will increase and the number of fibers will approximately scale with source power. Overall system efficiency, at best, will still be near 0.8% to 2% at a photovoltaic temperature of 260°C.

9.4 Photovoltaic Impedance Matching to Torque-Motor Load

An important assumption in the efficiency calculations of Table XV is that all the electrical power that can be supplied by the photovoltaic cell (or cell array) when illuminated is actually delivered to the load. In order for this to occur, each photovoltaic cell must be operating at the maximum-power point of its current-voltage (I-V) curve. Cell I-V characteristics change with temperature, and the load impedance will be a function of temperature and time. It is the job of an impedance matching device or circuit to continually establish matching at the highest efficiency possible, ideally 100%, to obtain overall system efficiencies listed in Table XV. The impedance matching system must be capable of operation between -54°C and 260°C at electrical powers of 5 mW to 5W (Figs. 9-6 and 9-7).

Assuming series and shunt resistance effects are negligible, the maximum electrical power output of the GaAs photovoltaic is affected principally by the change in output voltage with temperature. Between -54°C and 260°C, V_{mp} decreases from 1.0V to 0.45V, (Fig. 9-2). This dependence is expected regardless of source type although higher incident intensities will increase V_{mp} over the entire temperature range. Solar-cell data has shown that I_{mp} is relatively insensitive to temperature (Fig. 9-3a); the same is expected for a monochromatic source with a GaAs cell. Because the GaAs band-gap narrows with increasing temperature, lamps with appreciable near-infrared emission should show larger increases in I_{mp} as temperature increases (see Item I.A in Table XV). Since the cell output current is directly proportional to the incident photon flux, the cell I-V curve and maximum-power point will also change with fluctuations or intentional changes in the optical power output of the source(s).

An advantage of a low-frequency torque motor is that its operation is not overwhelmingly dominated by inductive reactance. Unlike some electrical loads, such as centrifugal motor armatures, the inductive reactance of a torque motor is not large enough to cause severe changes in the input impedance during start-run-stop cycles. Electrical matching of a power-by-light cell to a centrifugal motor load requires precise temporal matching during switching to provide a low-voltage high-current condition during start up and a high-voltage low-current condition during normal running. Alternative impedance matching techniques are available when using a torque-motor load.

The torque motor is a current sensitive device. Since the response of a servovalve in which it is mounted is flat above the rated current (voltage), it is only necessary to assure that voltage is above the rated operating point to realize a stable situation. The required voltage is determined largely by the positive temperature coefficient of resistance of the armature coil. If the room temperature resistance of the coil copper wire is R_{coils}, then resistances at -54°C and 260°C will be $0.68R_{coils}$ and $1.94R_{coils}$ respectively. In order to maintain rated current into the torque-motor coil if directly connected, the cell voltage would have to increase with temperature, not decrease as experimentally observed.

Examples of power-by-light cell requirements for selected torque-motor loads are shown in Table XVIII. For purposes of simplification, a solid-state laser diode has been chosen for use as the optical source. The type of torque-motor selected was one that was available in two-stage hydraulic servovalves. These required full-stroke current ranging from 4mA to 80 mA (~ 32 mW electrical power at room temperature). Optical power was supplied from individual solid-state sources so that each fiber optic line delivered 21.5 mW to the GaAs photovoltaic. With a maximum power-conversion efficiency of 21% at 260°C, then a maximum photovoltaic output of 4.5 mW (10 mA at 0.45V) is expected for each cell. This corresponds to a matched-power load resistance, R_{mp}, of 45 ohms per cell. In order to resistively match to the torque-motor coils at 260°C (parallel-aided configuration), 14 cells connected in series with the load would be required. Series connection of the cells is the simplest approach to meeting the voltage requirements of the torque motor. Summaries of cell requirements at <u>each</u> temperature for 10, 20, 40, and 80-mA coil currents are shown in Table XVIII. These currents require 1, 2, 4, and 8 optical fibers per photovoltaic cell. Since individual cell output voltage and power increase and coil resistance decreases as temperature is lowered, the fractional number of required series cells for matching over the temperature range decreases by about a factor of 6. Unless cells are removed from service or optical power is reduced by some other means at lower cell temperatures, overall system efficiency will be less than the calculated values of Table XV due to impedance mismatch. Eventually, in Table XVIII, as incident optical power increases, more electrical power can be provided by one cell (at lower temperatures) than is needed by the torque motor. At this point it therefore makes no sense to further increase optical power at the photovoltaic.

Impedance matching between source and load in a photovoltaic power system is generally accomplished by a dc-dc voltage converter, a device which can be thought of as a variable-turns-ratio dc transformer. The converter requires a logic circuit with signal inputs from sensing elements in the photovoltaic cell and load to work properly. The sensing elements monitor changes in

TABLE XVIII

POWER-BY-LIGHT CELL REQUIREMENTS WITH TORQUE-MOTOR LOADS

Optical Power Per Cell (mW)	T°C	V_{mp} Per Cell (Volts)	I_{mp} (mA)	R_{mp}* Per Cell (ohms)	R_{coils}** (ohms)	Required Number of Series Cells (***)	Required Output Voltage (Volts)
21.5	260	0.45	10.0	45	611	13.6 (14)	6.30
21.5	25	0.86	10.8	80	315	3.9 (4)	3.44
21.5	-55	1.01	10.4	97	214	2.2 (3)	3.03
43+	260	0.45	20.0	22	155	6.9 (7)	3.15
43	25	0.86	21.5	40	80	2.0 (2)	1.72
43	-55	1.01	20.9	48	54	1.1 (2)	2.02
86++	260	0.45	40.1	11	39	3.5 (4)	1.80
86	25	0.86	43.0	20	20	1 (1)	0.86
86	-55	1.01	41.7	24	14	0.6 (1)	1.01
172+++	260	0.45	80.3	6	9.7	1.7 (2)	0.9
172	25	0.86	86.0	10	5	0.5 (1)	0.86
172	-55	1.01	83.4	12	3.4	0.3 (1)	1.01

* $R_{mp} = \frac{V_{mp}}{I_{mp}}$

** Parallel-aided coil configuration

*** Next highest integer

\+ 2 fibers/cell

++ 4 fibers/cell

+++ 8 fibers/cell

maximum-power-point current and voltage and allow the logic controls to take corrective action on the dc transformer-turns ratio and re-establish the best impedance match. The approach to stabilizing power transfer in a generator-load pair is often referred to as maximum-power tracking.

In the examples of Table XVIII, a voltage converter has to be used with a current regulator to maintain torque-motor current at the rated value. The converter also has to be able to handle the factor-of-6 impedance mismatch over the temperature range of application. As temperature is changed, the voltage converter would establish best imedance match and change the level of optical power incident on the photovoltaic cells and generated primary current. In this way, the minimum optical power would be used at each temperature to operate the load, and efficiency values of Table XV could be approached. Of course, impedance matching and current regulation will require additional electrical power which must be factored into overall system efficiency. Furthermore, additional fiber optic feedback is required to change optical power sent to the photovoltaic array.

Solid-state dc voltage converters with efficiency as high as 95% are readily available for photovoltaic power systems operating at hundreds of volts and power levels of one kilowatt or more (Ref. 36). Special converters can be designed for systems at 24V levels at 100W (90% efficient) (Ref. 37). As output voltage and power decrease further, however, conversion efficiencies of commercially available voltage converters fall off rapidly. Developmental devices that will operate with efficiencies of 50%-85% at power levels below a few milliwatts and at voltages as low as 0.9V, have been reported (Refs. 38 and 39). High conversion efficiency was in part due to the use of capacitor networks instead of resistor networks to achieve bias control of individual devices. It must, however, be pointed out that only high-impedance loads ($\geq$ 100 kohms) were tested with this converter and power efficiencies decreased as the load impedance decreased. It remains to be seen if a similar kind of converter can be made to operate well with moderate-to-low-impedance loads as shown in Table XVIII.

A basic requirement of impedance matching in the power-by-light application of this study is that the circuit itself must operate over the -54°C to 260°C photovoltaic temperature range. This would require use of GaAs-based devices rather than the usual silicon or germanium devices. A special design and development effort on a voltage converter based on GaAs would be required to accommodate (1) both low and high-temperature operation (2) matching of low electrical powers (5 mW to 5W) at low voltage into relatively low-impedance torque-motor loads, (3) rapid response under pulse-width modulation (up to 2 kHz rate), and (4) high efficiency. In addition, optical feedback would require a high-temperature optical source, adequate coupling into a return fiber and added electronics at the control computer. A current regulator in the secondary circuit could also be constructed using GaAs devices.

Since photovoltaic current is not strongly affected for a given photon flux (especially for the solid-state sources) by temperature variation between -54°C and 260°C, and the required torque-motor current is temperature insensitive, an alternative power-shedding technique could be applied as the temperature was lowered from the 260°C matched condition. Using a switching network, one photovoltaic cell after another could be progressively disconnected and optical power turned off to the cells. This technique would require feedback using some kind of temperature sensor and optical fiber to the control computer which would then disconnect cells via additional fiber optic lines to photosensitive switches in the cell array. Alternatively, power-shedding logic incorporating GaAs devices could be on site and be separately powered by fiber optic lines. The control would be stepwise rather than continuous. As in the case of the dc-converter approach, implementation would add greatly to system complexity and cost, and additional efficiency factors would have to be included in overall system efficiency. Another possibility is photovoltaic array switching which would involve changing the cell configuration from full series to series-parallel and full parallel as the temperature is lowered. The required switching network in this case would be even more complex than that needed for power shedding.

From the preliminary survey into the question of full-temperature impedance matching between photovoltaic cells and torque-motor loads, implementation will require substantial development, be expensive, and will add considerable complexity to the power-by-light system. Centrifugal-type loads will require a converter approach that can quickly handle large inductive impedance swings. Torque-motor loads can also utilize a power-shedding scheme. The efficiencies of Table XV will be reached only if impedance matching and current regulation (if needed) is 100% efficient. In the next section another possibility for a power-by-light demonstration system using a torque-motor load is discussed.

9.5 Recommended Power-by-Light Demonstration System

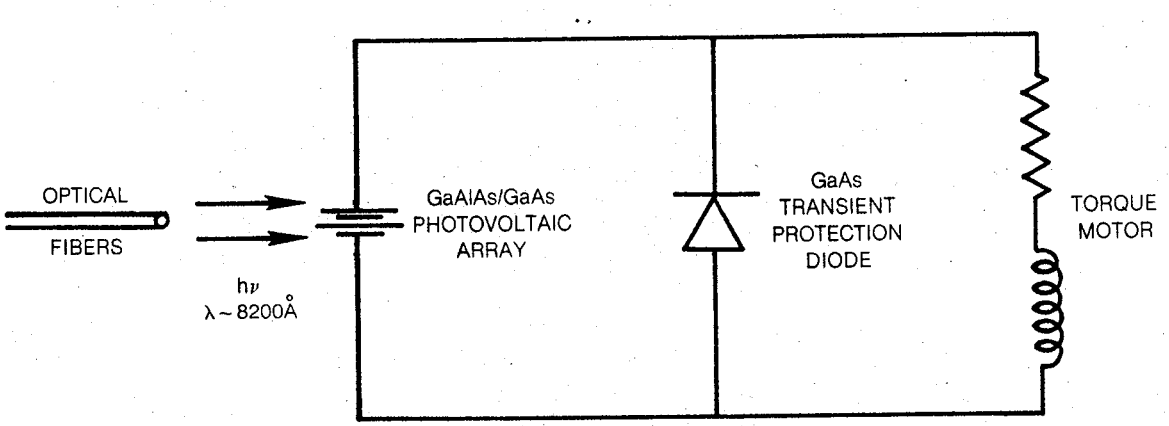
In order to achieve system efficiency and thereby reduce optical power requirements, a technique for establishing impedance match between photovoltaic and torque-motor load is required as temperature changes. This is necessary because photovoltaic output power (at a given optical flux) and required coil power change with temperature. Section 9.4 had addressed factors which must be considered in various impedance matching techniques for changing optical excitation and delivery to the photovoltaic based on cell characteristics and the needs of the load. Power-by-light system requirements are such that considerable increases in cost and complexity will result for contemplated impedance matching schemes. This section addresses the consequences on system efficiency of single-temperature impedance matching of a GaAs photovoltaic array to a torque-motor load.

Photovoltaic power output is at its lowest point at the highest application temperature, 260°C. This is due to voltage output. For the solid-state sources the generated current will be more or less fixed as a function of temperature by the optical power arriving on the cells. Because of GaAs bandgap narrowing, lamp sources are expected to produce larger increases in generated current as temperature increases. The torque motor requires a certain value of current for proper functioning, but could withstand a 150% overdrive in power without damage. Due to a positive temperature coefficient of coil resistance for the copper wire, maximum electrical power is required at 260°C. If the photovoltaic cell and torque motor are resistively matched at this highest application temperature, there will be sufficient power available at lower temperatures for operating the torque motor. Use can be made of the I-V characteristics of the cell at lower temperatures to prevent large current increases.

With no active impedance matching device placed between photovoltaic and load, these can be simply connected as in Fig. 9-8. A GaAs transient-protection diode is required to prevent inductive voltage spikes from damaging the cells. For purposes of illustration a torque-motor requiring 10 mA was selected as load along with individual laser-diode-coupled fiber optic lines, each capable of delivering 21.5 mW of optical power (λ = 8200 Å) to a photovoltaic cell (Table XVIII). Resistive matching at 260°C requires that 14 cells be connected in series to provide the 10 mA of current into a set of torque-motor coils (parallel-aided configuration). With the help of the Ref. 2 data in Figs. 9-2 and 9-3a and calculated photovoltaic power-conversion efficiencies for the laser diode source, photocell current-voltage curves have been sketched in Fig. 9-9 using the maximum-power point (x) and endpoints for each temperature. Also shown are the torque-motor demand lines at each temperature (coil inductance has been ignored). The intersection of each line and the corresponding I-V curve is the operating point for the cell. As temperature decreases from the 260°C matching point, the cell is placed in a more short-circuited condition by the coils. Although there is the possibility of 10-14V maximum-power voltage outputs at the lower temperatures, the loaded cell can only respond with sufficient voltage to maintain current near the rated requirements, i.e., the photovoltaic cell is in effect a current regulated power source. The slight current increase that is generated at lower temperatures will not pose an operational problem for the load. The overall effect of single-temperature matching at 260°C is that the higher cell efficiencies potentially available at lower temperatures by operating at the maximum-power points can not be realized.

Figure 9-10 summarizes power-by-light efficiencies if (1) 260°C is the ambient temperature at which the cell and torque motor are resistively matched and (2) cooling is not required at the ILD to maintain a maximum 35°C source temperature. The efficiency of optical generation and delivery to the photovoltaic can be as high as 4.5% or 9% depending on whether one or two fibers

RECOMMENDED POWER-BY-LIGHT DEMONSTRATION CONFIGURATION

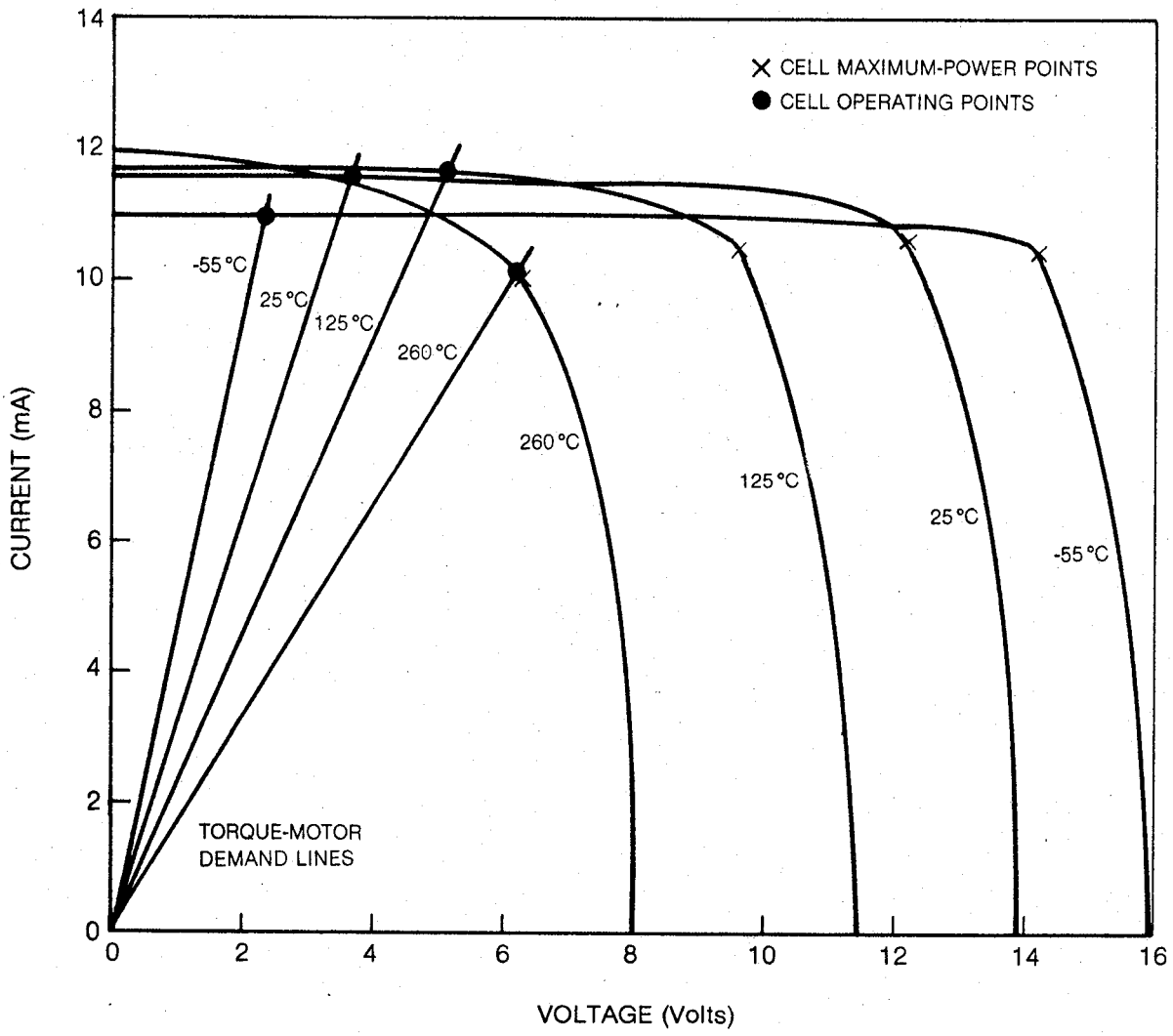


82-12-2-4

FIG. 9-9

GaAs PHOTOVOLTAIC AND TORQUE-MOTOR CHARACTERISTICS (I)

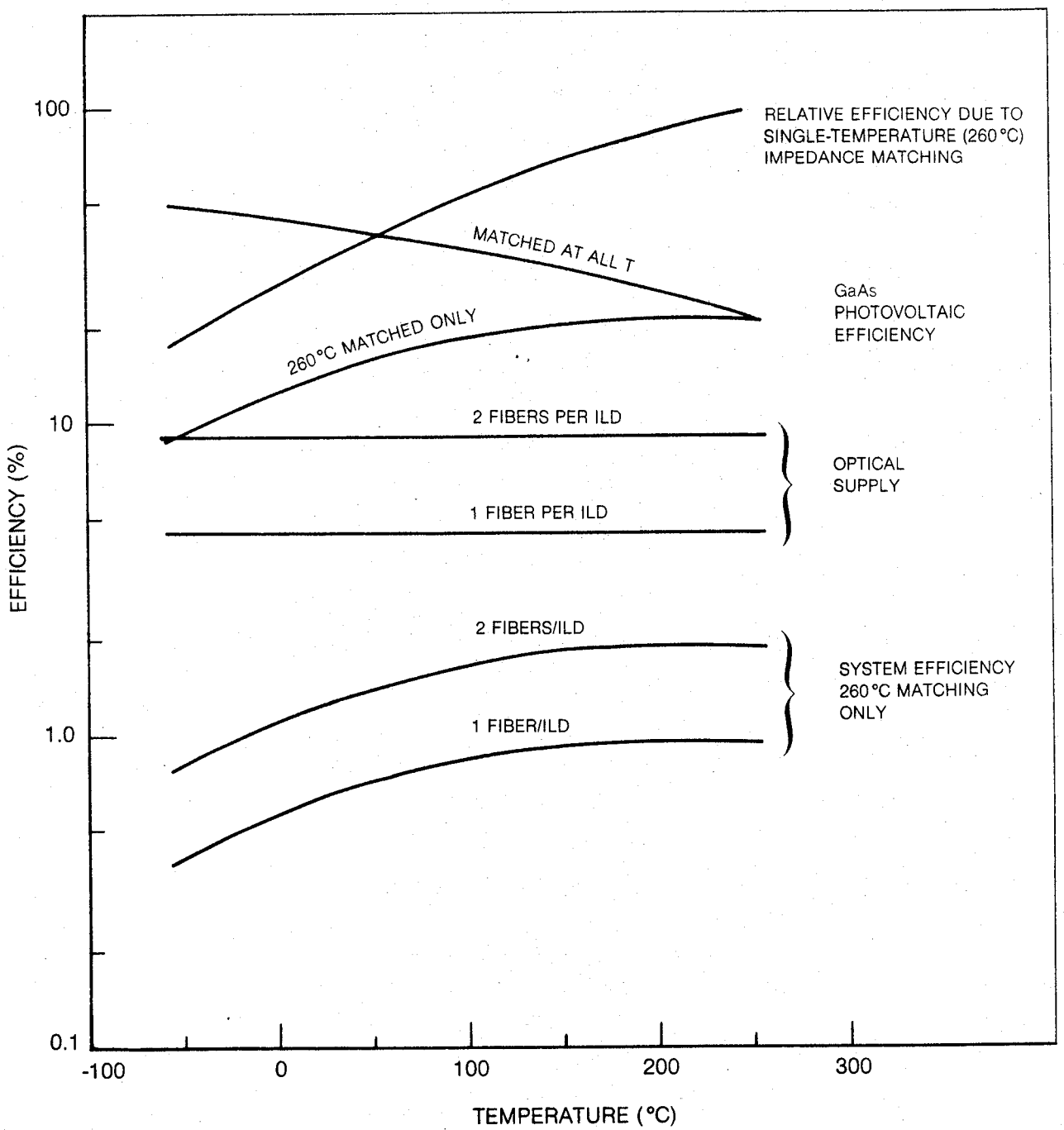
14 CELLS IN SERIES
21.5mW ILLUMINATION (8200Å) FOR EACH CELL



82–10–9–5

POWER-BY-LIGHT EFFICIENCIES (I)

260 °C — MAXIMUM PHOTOVOLTAIC AMBIENT TEMPERATURE
35 °C — MAXIMUM ILD AMBIENT TEMPERATURE



82-12-2-2

are coupled to each ILD. The maximum anticipated photovoltaic efficiency is shown for the case where operation is at the cell's maximum-power point over the entire temperature range; i.e., if the cell and load could be matched at all temperatures without utilizing any additional electrical power. The uppermost curve shows the temperature dependence of an efficiency factor resulting from single-temperature matching and reflects the ratio of the cell operating current-voltage product to the maximum electrical power available from the cell. The overall photovoltaic efficiency is the product of these two factors and is shown in the figure and also given in Table XIX. The lower curves combine optical supply and resulting photovoltaic efficiency for the case of single-temperature matching. For an ILD with two coupled fibers, system efficiency should increase from 2% at 260°C to 4.6% at -55°C; however, with single-temperature matching, system efficiency would fall a factor of 2.5 to 0.8% at -55°C. The factor-of-six resistance mismatch over the temperature range shows up as a factor-of-six lower system efficiency at -55°C compared to that possible if full-temperature (and lossless) impedance matching were in effect.

It is important to note that if a GaAs dc-dc converter could be developed for high and low-temperature use, its efficiency would have to be greater than 45% over the entire temperature range to offer an overall improvement in performance over single-temperature resistance matching. Under this condition, the cell power-conversion efficiency multiplied by converter efficiency would be 9 to 22%, the same range (but in reverse order) as for matching only at 260°C (last column of Table XIX).

A significant reduction in the number of required series cells and increase in system efficiency at lower temperatures will result if the maximum allowable photovoltaic temperature is reduced from 260°C. If the photovoltaic is fuel-cooled so that its temperature does not exceed 150°C, calculations similar to those shown in Figs. 9-9 and 9-10 can be made for single-temperature matching at 150°C. Table XX summarizes conditions for single-temperature resistance matching for these two cases. The most notable effect is that the required number of GaAs photovoltaic cells has decreased from 13.6 (or ~ 14) to 7.3 (or ~ 7). In Fig. 9-11, the expected current-voltage curves are shown between 150°C and -55°C along with torque-motor demand lines. Figure 9-12 shows the effect of single-temperature matching at 150°C. The efficiency factor (upper curve) only decreases about a factor of 3 compared to the factor of 6 for 260°C matching. With respect to overall system efficiency, significant improvement is observed at 150°C (about 50%) and -55°C (about 100%) compared to Fig. 9-10. The reduction in the number of optical lines from 14 to 7 is an attractive feature of restricting photovoltaic cell temperature to 150°C and below. A small bonus is also gained in reduced photovoltaic diameter in this case.

TABLE XIX

POWER-BY-LIGHT EFFICIENCIES USING ILD SOURCES

Item	T(°C)	Impedance Matched At All T (%)	Resistance Matched At 260°C Only (%)
(a) GaAs Photovoltaic Power Conversion Efficiency	260	21	21
	125	33	19.9
	25	43	14.1
	-55	49	8.6
(b) System Efficiency	260	2.0 (1.0)*	2.0 (1.0)
	125	3.1 (1.5)	1.9 (0.95)
	25	3.9 (1.9)	1.3 (0.65)
	-55	4.6 (2.3)	0.8 (0.4)

( )* -one fiber (f) per ILD

TABLE XX

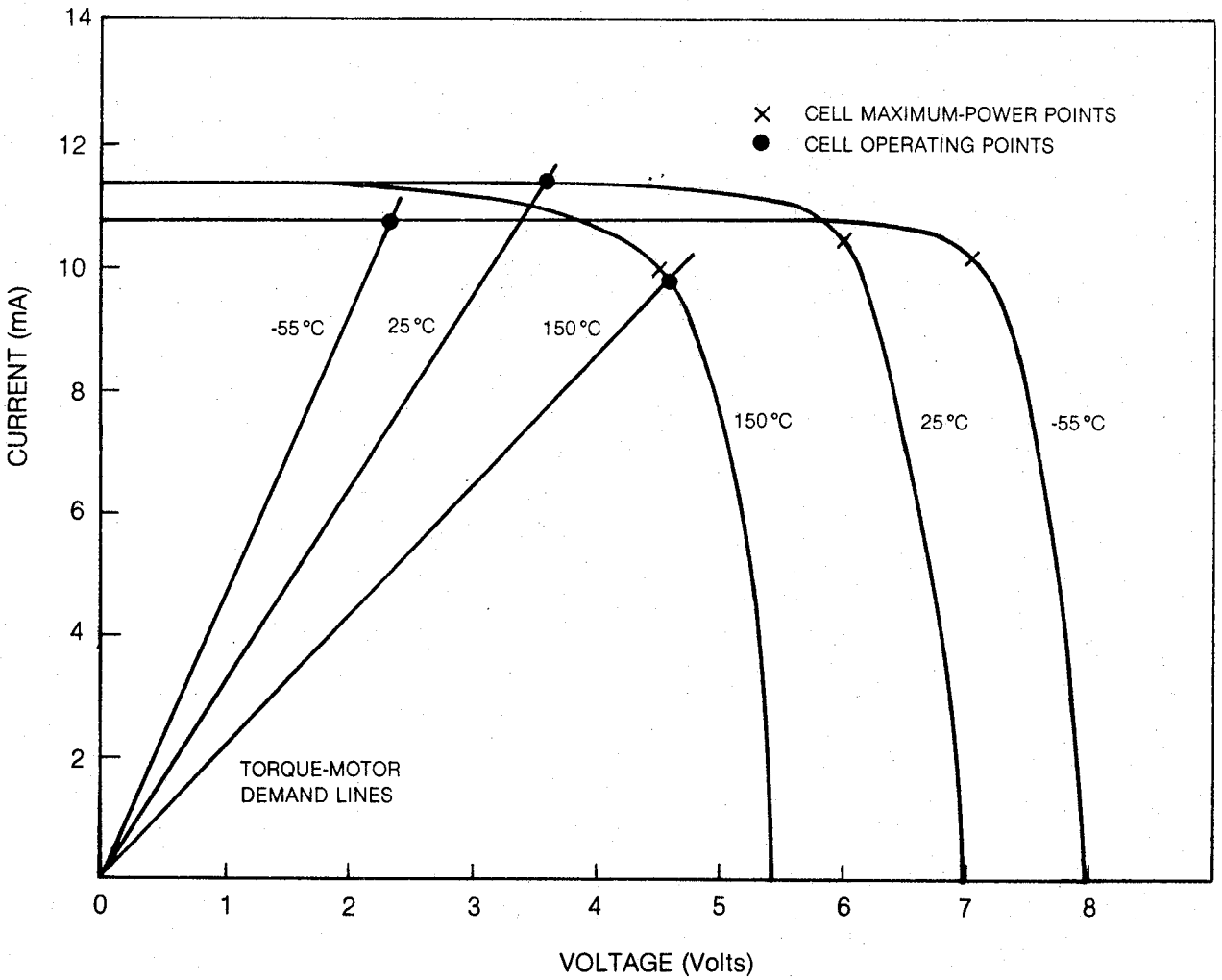
CONDITIONS FOR SINGLE-TEMPERATURE RESISTANCE MATCHING OF GaAs PHOTOVOLTAIC CELL TO TORQUE MOTOR

	Maximum Ambient Photovoltaic Temperature	
Matching Temperature :	260°C	150°C
Required Current :	10 mA	10 mA
DC Resistance of Coils :	610 Ω	470 Ω
Number of Series GaAs Cells :	14	7
Incident Optical Power per Cell (λ = 8200Å) :	21.5 mW	21 mW
Voltage Output Per Cell		
Open Circuit :	0.58 V	0.77 V
Maximum Power :	0.45 V	0.64 V
Suggested Cell Diameter (Based on R_S = 0.04 ohm-cm^2 at 25°C) :	2 mm	1.5 mm

FIG. 9-11

GaAs PHOTOVOLTAIC AND TORQUE-MOTOR CHARACTERISTICS (II)

7 CELLS IN SERIES
21mW ILLUMINATION (8200Å) FOR EACH CELL

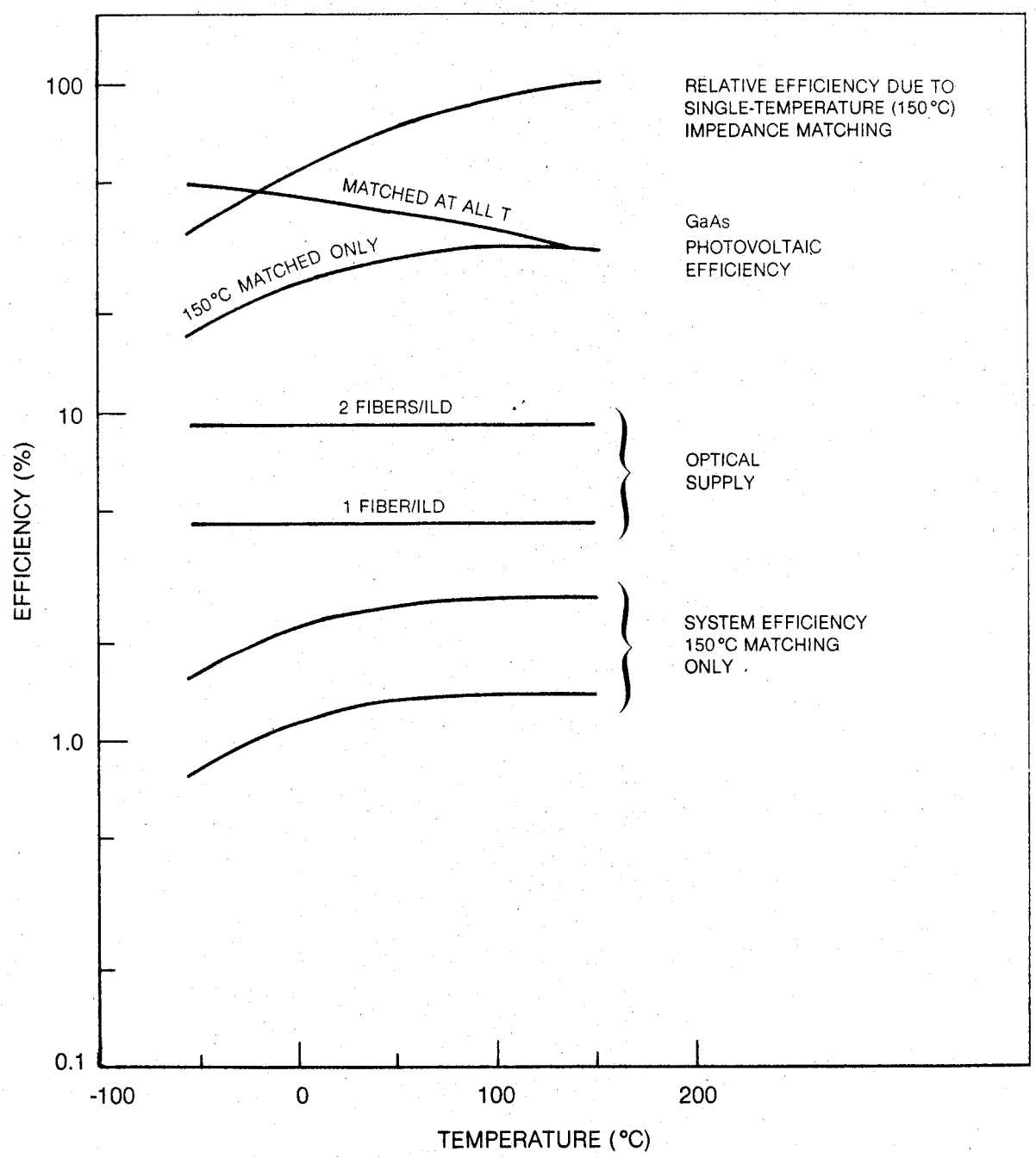


82-12-2-1

FIG. 9-12

POWER-BY-LIGHT EFFICIENCIES (II)

150 °C — MAXIMUM PHOTOVOLTAIC AMBIENT TEMPERATURE
35 °C — MAXIMUM ILD AMBIENT TEMPERATURE



82-12-2-3

Up to this point, no consideration has been given to the effects of torque-motor inductance on the switching characteristics of the photovoltaic array. When cells and load are directly connected as in Fig. 9-8, at the instant the cells are activated, a large inductive reactance will be present which will impede current flow. The situation is illustrated in Fig. 9-13 for the simple case of an inductor and series resistance representing a torque motor with $L_{coils} = 0.015\ R_{coils}$. For purposes of illustration, the ac cell resistance was assumed to be small compared to R_{coils}. For several time constants after initialization of the light pulse, photovoltaic output current will increase and approach the dc torque-motor demand current, in this case I_{mp}. Since array power output during the transient is not at its maximum value, $I_{mp}V_{mp}$, system efficiency will be less than predicted and will depend on the value of time constant and the duration of the pulse.

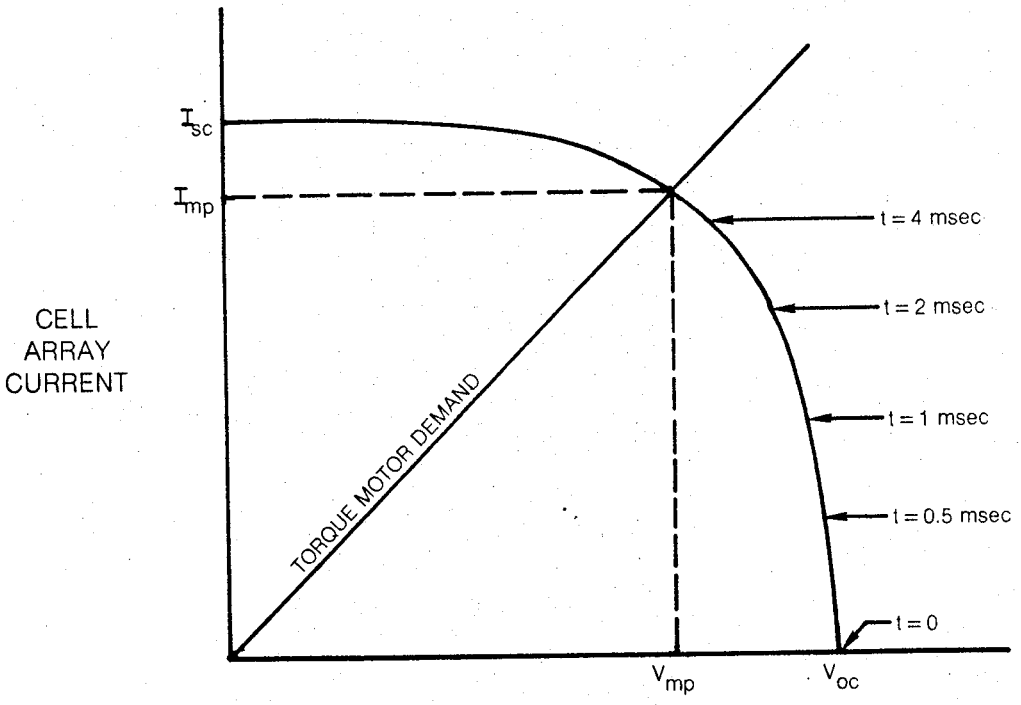
In conclusion use can be made of single-temperature resistance matching of torque motor to photovoltaic at 260°C and the built-in current regulation of the photovoltaic to demonstrate power-by-light switching down to -55°C. This technique offers the advantages of reasonable performance, low cost, simplicity, and greater reliability compared to more complicated impedance matching or power-shedding techniques. For a system using laser diode sources, the overall system power-conversion efficiency, that is electrical in at optical sources to electrical power consumed at the torque motor, will be at most in the range, 0.4 to 2%. This does not include source cooling or optical-power-supply efficiency.

9.6 Suggested Areas for Future Work on Power-by-Light

A summary of power-by-light efficiencies using a semiconductor laser source was shown in Table XV. In the optical power generation and delivery train, the lowest efficiency factor occurs at the source. The laser diode source was selected for power-by-light control application because of the long lifetime, high efficiency of coupling to individual fibers, and high system efficiency under pulsewidth modulation. The ILD E→O power-conversion efficiency is not expected to improve much above about 20% for a high-power source. As GaAs and related Group III-V technology advances, progress will be made in increased LD optical power output and temperature of operation. Higher optical output is important for generating increased electrical current in the load. Such sources (quantum-well structures) will be commercially available in the very near future. Higher LD operational temperature is important for increased efficiency because the listed laser diode would have to be cooled to less than 35°C (if the ambient temperature were higher) in order to preserve the 10,000-hour lifetime. If a maximum ambient temperature of 125°C is specified for the laser diode, a three-stage thermoelectric cooler is estimated to be about 12% efficient in removing internally generated heat

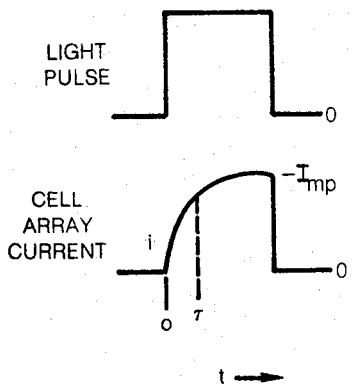
FIG. 9-13

PHOTOVOLTAIC DYNAMICS WITH TORQUE-MOTOR LOAD



$$i = I_{mp}(1 - e^{-\frac{\tau}{t}})$$

$$\tau = \frac{L_{coils}}{R_{coils}} = 1.5 \text{ msec}$$



83-3-119-35

from a thermally insulated ILD placed in this ambient. Two specific areas for future work would be (1) development of an efficient method for cooling the laser diode source (e.g., a microelectronic refrigerator) and (2) development of technology for higher-temperature LD operation with good efficiency at high-power levels.

As GaAs III-V semiconductor device technology advances, there is the possibility that shorter-wavelength solid-state sources can be used in a power-by-light application. An advantage in using such an optical source matched to a shorter-wavelength photovoltaic is that higher voltage output is possible due to the larger band gap of the absorber. Also, it is possible for the percentage change in output voltage with temperature to be less with a higher-band-bap photovoltaic. This would lead to a smaller percentage change in load resistance with temperature for operation at the PV maximum-power point. Balancing these trends is the trend that short-circuit current density will decrease with increasing band gap. The product of open-circuit voltage and short-circuit current defines the upper limit of power extraction from a PV cell. Pushing high-power solid-state laser operation to wavelengths below 7500Å will be a difficult task. This is due principally to much more difficult materials technologies associated with candidate Group III-V ternary and quaternary materials. Even with a 7500Å emitter and a matched photovoltaic, only about a 0.1V increase in V_{mp} and a 0.1-factor increase in photovoltaic efficiency at 260°C are expected compared to an 8200Å emitter and a GaAs absorber. Shorter wavelengths would bring additional benefits; however, the probability of fabricating visible high-power solid-state lasers in the short term is extremely low. Any additional work on solid-state sources is best spent on developing present 8200Å emitters so that they can operate at higher optical output and/or higher ambient temperature. Another negative factor in implementing shorter-wavelength optoelectronics is that glass fiber losses increase strongly with decreasing wavelength. At 6000Å, attenuation in silica fibers is a factor of 2.3 higher than at 8000Å and at 4000Å it is nearly a factor of twenty higher (Ref. 18). On the other hand, the relatively short distances typical of aeronautical power-by-light systems and the low attenuation to begin with would not make fiber losses of serious concern unless wavelengths were well below 6000Å.

The highest power-by-light system efficiency is obtained for the laser diode and matched photovoltaic converter. The laser diode considered in Table XV can emit 120 mW of optical power at 8200Å using both diode facets. The electrically generated optical power must be transmitted and converted back to electrical power. Optical-to-electrical conversion efficiency at the photovoltaic will probably not exceed 25% at 260°C or 50% at -54°C. After fiber coupling, fiber transmission, and PV cell conversion, the electrical power available to the load is down to 12 mW (two coupled fibers) at 260°C. Even with possible advances in ILD output power by an order of magnitude, a single

channel (source, fiber and PV cell) will be limited to approximately 60 mW of matched electrical power to the load. If load powers in excess of a few watts are required, use will have to be made of lower-efficiency lamp sources. Due to having to operate the lamps and photovoltaic continuously, a large system efficiency penalty results under pulsed operation. If this penalty is acceptable, additional work on lamps and coupling to optical fibers is suggested. It would be interesting to demonstrate whether the values in Table XV and Figs. 9-6 and 9-7 for the arc and W-X_2 lamps can be experimentally reached. Future work could involve (1) improvement in the lifetime of the lamps, (2) optimization of the spectral output of the arc lamp to more closely match the GaAs photovoltaic, (3) optimization of lamp geometry for high-efficiency and uniform coupling into fiber bundles, (4) design of appropriate cooling of the lamps on aircraft, and (5) development of techniques for coupling a large fiber bundle to a photovoltaic cell for operation between -54°C and 260°C. Of particular relevance for a lamp-based power-by-light system would be electrical storage over the operating temperature range. This would reduce the duty-factor penalty since electrical power not switched to the load could be stored and used at a later time. A suitable storage system is not presently available for operation between -54°C and 260°C.

At load powers in excess of 10 watts, the fiber optic bundle becomes too large to be practical using lamp sources. New ways to utilize the optical energy directly, or in the form of heat, may possibly provide higher efficiency and a simplier system or allow use of higher-power sources. One approach would be to consider use of coherent sources capable of much higher coupling of optical power into a fiber. Sources such as CO_2 lasers are attractive in this respect. Photomechanical effects are known but have been little studied, and those that have been studied appear to be very weak. Thermomechanical effects are, however, well known and well understood. In addition, optical energy can generally be converted into thermal energy with high efficiency. If one could develop a thermomechanical actuator instead of an electromechanical one, an infrared power-by-light system built around a 10.6-μm CO_2 laser source might be feasible. One noteworthy advantage would be freedom from impedance matching, either temperature or load induced. A serious drawback is that special infrared fibers are required. Infrared fibers are non-silica based and are constructed from materials such as $ZnCl_2$, TlBrI, and KCl which are much more difficult to fabricate into fibers and use than fused silica. Protection from moisture is an important consideration. Present-day fiber attenuation is high; however, there is the promise of much lower attenuation in the future. A further problem is that some form of compensation would have to exist at the thermomechanical actuator to differentiate between thermal changes caused by laser radiation and changes caused by a varying ambient temperature. Another possibility to utilize CO_2 laser derived thermal energy would involve thermoelectric generators; however, existing thermoelectric power converters suffer from low efficiency (a few percent) at elevated temperatures.

The calculated photovoltaic efficiencies in Table XV can be achieved if impedance matching to the intended load is established and there is no expenditure of power in the matching circuit. Presently, there is no efficient way of impedance matching at power levels of 5 mW to 5W using a low-impedance photovoltaic over the -55°C to 260°C range. Special circuitry and use of GaAs devices would be required in a dc-dc converter and current-regulator approach. Such matching would be an absolute necessity for centrifugal armature-type motors. Torque motors may utilize laser-diode power shedding or electrical storage as photovoltaic temperature decreases. Implementation of these techniques will add significantly to system complexity. A demonstration system that utilizes direct connection of cell array to torque-motor load and impedance matching at the highest temperature will lead to decreased low-temperature efficiency compared to predicted values. This approach has the advantages of simplicity and reasonable performance. Whether continuous or stepwise impedance matching would be more efficient (and at what price in complexity) constitutes an area of study and development.

10.0 SUMMARY OF RESULTS (PARTS I AND II)

This report described work aimed at advancing the use of fiber optics and GaAs high-temperature photoswitch devices for aircraft control systems. The program was divided into two parts: (1) a developmental program for design, fabrication and testing of GaAs devices for demonstration of fly-by-light switching between -54°C and 250°C; (2) a follow-on feasibility study program on power-by-light and improved fly-by-light designs for pulse-width-modulated fiber optic switching of actuator loads. GaAs is better suited for higher-temperature operation compared to silicon because of its higher energy gap. The ability to operate at higher temperatures will lead to reduction or elimination of system cooling requirements for a photoswitch system based on GaAs devices.

In the hardware part of the program, the breadboard photoswitch circuit utilized the following GaAs high-temperature devices: (1) a heterojunction phototransistor (the photosensitive element), (2) a junction field-effect transistor (JFET) (the power switch) and (3) a junction mesa diode (transient-protection device). The phototransistor was chosen because it could exhibit gain (and therefore reduce optical source requirements) and it was readily fabricated using existing GaAs technology. The JFET device was used because it had a proven record of high-temperature testing at United Technologies Research Center and was compatible with pulse-width modulated switching. The optical path consisted of a high-radiance infrared-emitting diode (λ=8360Å) coupled to an optical fiber, two optical connectors, a transmission cable (10 meters), and a fiber optic pigtail for delivering optical power to the GaAlAs/GaAs phototransistor. High-temperature gold-germanium eutectic brazing to a metallized optical fiber was used in the process for hermetic fiber sealing within the phototransistor package.

For demonstration of optical switching, the phototransistor was placed in parallel with the gate of the JFET power switch. When illuminated, the phototransistor exhibited gain and generated sufficient photocurrent (about 1.3 mA through a 10K resistor) to reduce JFET gate voltage and switch current into a torque-motor load. The photoswitch system was able to switch up to 100 mA of current with a stand-off capability of 20V. For optical switching over the -54°C to 250°C range, the required minimum infrared emission from the optical fiber inside the phototransistor package was 240 µW to 510 µW. If allowance were made for an extra 50% safety factor for operation and for losses in the optical path, then 650 µW to 1400 µW of optical power had to be coupled into the fiber at the infrared-emitting diode. If other available phototransistors with higher gains had been packaged, optical requirements could have been reduced by a factor of two. Each of three sets of GaAs photoswitch devices was operated over the specified temperature range and at 250°C for two hours at 50% duty cycle at 40 Hertz.

In the follow-on study effort on fly-by-light designs, the same high-temperature photoswitch design as demonstrated in the hardware phase was explored further. Improvements could be made to either increase the electrical power switched to the load compared to the demonstrated capability (100 mA at 20V, or 2W) or simplify the photoswitch circuit for switching at near the same electrical power for greater system reliability. In both cases the GaAlAs/GaAs phototransistor remained the key photosensitive device. For switching up to 0.5A to 1A (10-20W) into a load, higher-current-capability GaAs JFET's could be used in the delivered system. For optical control of higher electrical powers (e.g., 6A, 70W) bipolar transistors, similar in epitaxial-layer construction to the phototransistor, could replace the JFET power switch. For simplification of the present fly-by-light circuit, the phototransistor-JFET pair could be replaced with a higher-gain phototransistor with the option of using higher optical power for activation. Single phototransistors could be constructed for switching up to 0.2A (2.6W) or up to 0.5A (0.75W). The GaAs transient-protection diode would still be required due to the inductive load.

For a power-by-light system the electrical power required at the torque-motor must be generated as optical power and transmitted via optical fiber(s) to a photovoltaic array for conversion to usable electrical power. GaAs was chosen for study as the photovoltaic material because of (1) its high energy band gap, which leads to higher output voltage per cell compared to silicon, and (2) the high technological level which allows fabrication of efficient concentrator solar-cell structures. High system efficiency reduces source optical-power and cooling requirements. The factors which impact system efficiency and which were addressed during the study effort on power-by-light were optical power generation and transmission, photovoltaic design and power-conversion efficiency, and photovoltaic impedance matching to the torque-motor load. Electrical storage was not considered due to lack of a system which could function adequately between -54°C and 260°C.

Optical sources for power-by-light application can include solid-state emitters and lamp sources like arc and tungsten-halogen lamps. The injection laser and infrared-emitting diodes can be easily switched on and off in fractions of a microsecond, if necessary, and are directly applicable to pulsed-width-modulation actuator control. The lamps would have to be operated continuously and would require an additional fly-by-light optical line and photoswitch for control of current in the torque-motor circuit. This would be a more complex arrangement and without an energy storage capability would be less efficient. Coupling of infrared optical power from each injection-laser facet is readily accomplished with a single optical fiber. In order to approach their maximum efficiency, the lamp sources and infrared-emitting diode must be coupled to a fiber bundle with the help of external lenses. Two fiber types were considered: (1) a soft-glass fiber (core diameter = 200 μm, numerical aperture (NA) = 0.55); (2) a quartz fiber (core diameter = 1000 μm,

NA = 0.3). For the selected lamps the fiber bundle consisted of several-tens to several-thousands of optical fibers. Calculations were made of the efficiency of generation and delivery of usable optical power to a GaAs photovoltaic absorber for the matched high-power solid-state sources and for representative xenon short-arc and 3200°K tungsten-halogen lamps. Accounts were taken of electrical-to-optical power conversion at the source, coupling to the fiber(s), 10-meter fiber transmission, and loss through two connectors for each optical path. The highest efficiency, 9%, occured with the laser diode source. The other sources (and efficiencies) were infrared-emitting-diode (5%-7%), tungsten-halogen lamps (3%-6%) and arc lamps (2%-5%). Although the laser diode system was most efficient, it could only deliver 30 mW per fiber to the photovoltaic. The largest amount of optical power per fiber was for the case of a 300W arc lamp coupled into a 1000-μm fiber (210 mW at -54°C photovoltaic temperature to 280 mW at 260°C). This increase with temperature results because a greater percentage of lamp output is usable by the photovoltaic as the GaAs band-gap energy decreases with temperature.

GaAs concentrator solar-cell design is particularly suitable for a high-temperature power-by-light photovoltaic. The best design has a P/p/n epitaxial-layer (heterostructure) configuration. Internal cell series resistance is an important factor in determining cell fill factor, power-conversion efficiency and restrictions on the optical density that can be incident on the photovoltaic. For solid-state rather than solar sources, some minor changes in ternary layer composition and thickness or front-contact grid spacing can be made to produce lower cell series resistance or to expose more photosensitive area compared to the solar cell.

Photovoltaic optical-to-electrical power-conversion efficiency for wavelengths shorter than the GaAs absorption edge decreases with increasing temperature principally because of decreased cell output voltage. The maximum-power voltage decreases from 1.00V at -54°C to 0.45V at 260°C. The best photovoltaic power-conversion efficiencies are obtained with matched-wavelength solid-state sources. At 8200Å wavelength, expected efficiencies at the cell maximum-power points are 49% (-54°C), 43% (25°C) and 21% (260°C). For the lamps there is a spectrum of wavelengths below the GaAs absorption edge; therefore, photovoltaic efficiency for usable photon energies is necessarily less than for the matched-wavelength case.

System efficiency (electrical input at the source compared to electrical output at the photovoltaic) is highest for the case of the injection laser diode (2% at 260°C). Best efficiencies at 260°C for the other cases are 1.55% (infrared-emitting diode), 1.1% (tungsten-halogen lamp) and about 0.8% (xenon arc lamp). System efficiency for the solid-state sources continually decreases as temperature increases from -54°C. Because of the increase in

usable photons from the lamp sources as GaAs temperature increases, the system efficiency for the lamps increases slightly between -54°C and room temperature before decreasing at higher temperature. On the basis of maximum electrical power that could be generated at the photovoltaic due to coupling of one fiber to any of the selected sources, the laser diode is the best when using the 200-μm-diameter fiber (6 mW/fiber at 260°C). The use of a single 1000-μm fiber and 300W arc lamp can cause 47 mW of electrical power generation at the photovoltaic. A similar-wattage tungsten-halogen lamp would produce about a factor-of-8 lower photovoltaic electrical power per fiber optic line compared to the arc lamp.

In selecting a source for a particular power-by-light application, consideration must be given to system efficiency (including a duty-factor penalty for the lamps), photovoltaic power level, source lifetime, source cooling requirements and power-supply efficiency, and system costs. Experimental difficulties, particularly with optical coupling, management of fiber bundles, and matching of optical power to series photovoltaic arrays must also be carefully considered. For up to about 200 mW photovoltaic power, laser diode systems are preferred. With expected future advancements in laser diode output power (modulation-doped structures), laser diode system applicability could extend to 1W or 2W photovoltaic power. If higher electrical powers are required, the arc lamp would have to be used.

Calculated photovoltaic efficiencies are attainable only if each cell of the array is operating at the maximum-power point of its current-voltage curve with respect to the torque-motor load. As temperature changes, the power demands of the load and generating capability of the photovoltaic array change. As a result, some impedance matching device or circuit is required to re-establish matched conditions as well as regulate current to the torque motor as temperature changes. Conventional photovoltaic impedance matching utilizes the approach of maximum-power tracking using a dc-dc voltage converter placed between cells and load; however, there is no available system that can be used in the power-by-light application considered here. Such a converter would have to (1) operate between -54°C and 260°C, (2) match at low electrical powers (5 mW to 5W) at low voltages into relatively low-impedance loads, (3) have frequency response capability up to 2 kHz, (4) handle up to a factor-of-6 resistance mismatch over the temperature range, and (5) have high efficiency. Optical feedback to the control computer would also be required to change optical power sent to the photovoltaic cells. A torque-motor current regulator capable of full-temperature operation would also be necessary. Presumably, an impedance-matching system and current regulator which utilized GaAs devices could be developed for power-by-light use. A technique for coarse impedance matching is power shedding. In this case, optical sources could be turned off and cells removed from the array one by

one as temperature was lowered. Implementation of any active impedance-matching technique will greatly increase system cost and complexity. Also, additional electrical power would have to be generated at the photovoltaic to operate the impedance-matching circuitry and resident optical source for fiber optic feedback to the computer.

In view of the difficulties associated with full-temperature impedance matching, another option investigated was to resistively match photovoltaic and torque motor at a single temperature, 260°C. At this temperature power demand by the torque motor is at its highest value and photovoltaic output is at its lowest. As temperature is lowered, the cell current-voltage characteristics could provide some degree of current regulation for the torque motor. This is especially true for the nearly monochromatic sources. For an 8200 Å laser diode source, system efficiency would decrease from 2% at 260°C to 0.8% at -54°C. This is in contrast to an expected increase in efficiency to 4.6% if impedance matched at -54°C. The simplicity of this approach is such that a near-term demonstration of power-by-light for low-frequency torque-motor control at up to 260°C would be possible.

APPENDIX I

BREADBOARD DESCRIPTION

A requirement in Part I of this program was delivery of breadboard apparatus to demonstrate optically activated switching of current into a torque-motor load. The hardware delivered to NASA employed GaAs devices which could operate without the benefit of cooling at up to 250°C. Most of Part I of this report is devoted to discussions on the GaAs devices required to accomplish this task. This section describes the essential items of the breadboard. The actual testing procedures and results are described in Section 6.0.

The demonstration hardware consisted of three major items: (1) a table-mounted test rack which contained the necessary electronics and fiber optics, (2) the photoswitch probe assembly, and (3) three sets of GaAs high-temperature photoswitch devices. A two-meter long wire harness connected the breadboard to the probe assembly, which could be inserted into an oven or environmental chamber.

A front panel photograph of the test rack is shown in Fig. A-1. The following items were mounted on the test rack:

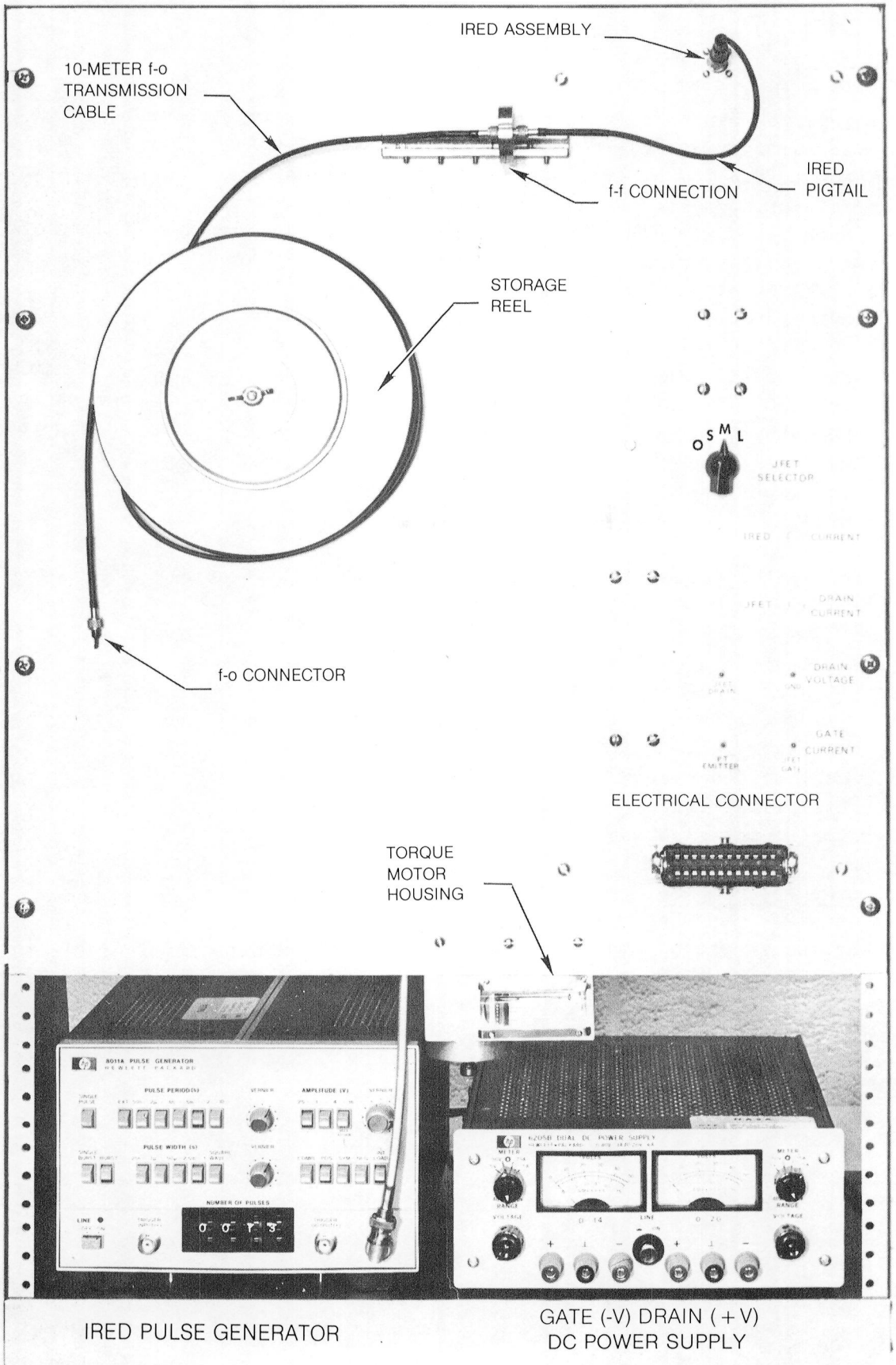
1. Pulse generator for the InfraRed Emitting Diode (IRED).
2. IRED in UTRC mount and fiber optic (f-o) pigtail.
3. Transmission optical cable with f-o connectors.
4. Storage reel for f-o cable.
5. Dual dc power supply for JFET gate and JFET drain.
6. Electrical circuitry for optical switching.
7. Torque-motor subassembly in housing.

1. Pulse Generator

The pulse generator could deliver up to 320 mA into a 50-ohm load. The breadboard IRED required up to 100 mA of current which was easily supplied from the pulse generator. Frequency (0.1 Hz to 20 MHz) and pulsewidth (25 ns to 100 ms) were adjustable as desired. The photoswitch devices were tested at 40 Hz and 50% duty cycle. The unit was equipped with a pulse-burst mode to deliver a preset number of pulses to the IRED.

FIG. A-1

FRONT PANEL OF PHOTOSWITCH BREADBOARD



82–198

82–6–103–1

2. IRED (D2)

The IRED emitted radiation at 8360Å. Maximum operating current was 200 mA but less than half was required for sufficient optical output to operate the GaAs photoswitch devices. The IRED was soldered into a brass housing which was mounted onto the breadboard panel. Electrical connection to the pulser was made using a teflon connector (J3) to the device package leads on the back side. A protection diode (D1) was placed across the IRED to protect against negative voltage transients. A pigtail arrangement for coupling optical output from the IRED into the breadboard transmission cable was made by epoxying a polished optical fiber at a position 20 μm above the dome of the IRED. A calibration curve for the optical power output versus drive current for this IRED is shown in Fig. A-2. The data were obtained by measuring the optical power output from the breadboard transmission cable plus another 3-meter cable and connector to simulate the phototransistor pigtail. The measured values were the best estimate of the optical power emission from the fiber inside each phototransistor package.

3. Fiber Optic Cable and Connectors

The optical cable and connectors were located on the front side of the breadboard rack. The panel optical path consisted of IRED, IRED pigtail, connector sleeve, 10 meters of transmission optical cable, and connector sleeve for connecting to the phototransistor pigtail.

4. Storage Reel

The ten meters of optical cable were wrapped around a plastic reel on the front panel for storage.

5. Dual dc Power Supply

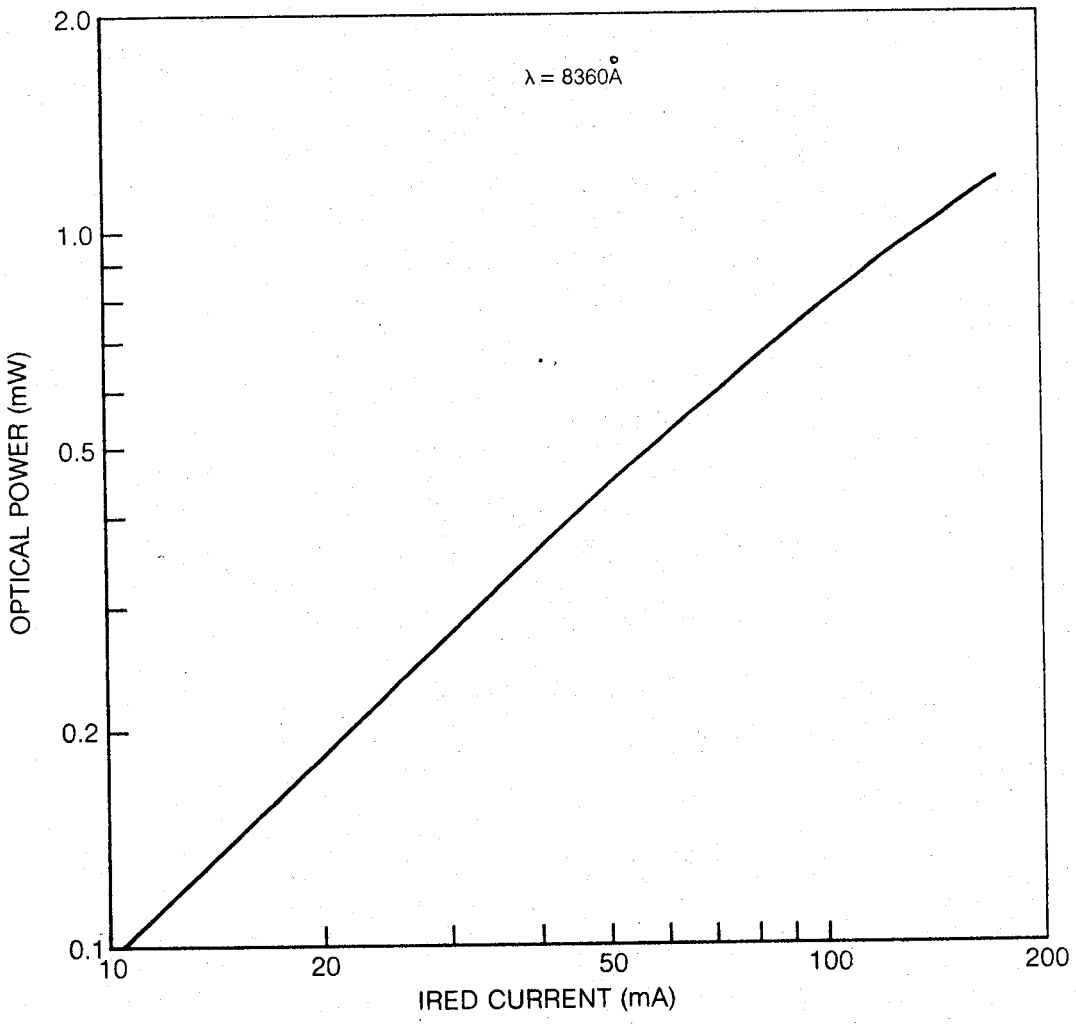
This power supply provided both JFET gate voltage (left side of supply) and JFET drain voltage (right side). Breadboard operation required -12 to -13V on the JFET gate (depending on device) and about +18V on the JFET drain to provide 80-mA rated current to the torque-motor coils and load resistor (R3).

6. Electrical Circuitry for Optical Switching

The circuitry for optical switching was located on the back side of the panel. A ribbon connector (J1) on the lower right side of the front panel provided contact to the probe assembly by way of an intermediate extension harness. The breadboard circuit diagram is shown in Fig. A-3, and listings of principal electronic parts and J1 pin designations are shown in Tables A-I and A-II.

FIG. A-2

OPTICAL POWER AVAILABLE TO THE PHOTOTRANSISTOR USING THE BREADBOARD IRED



83–3–119–34

BREADBOARD CIRCUIT DIAGRAM

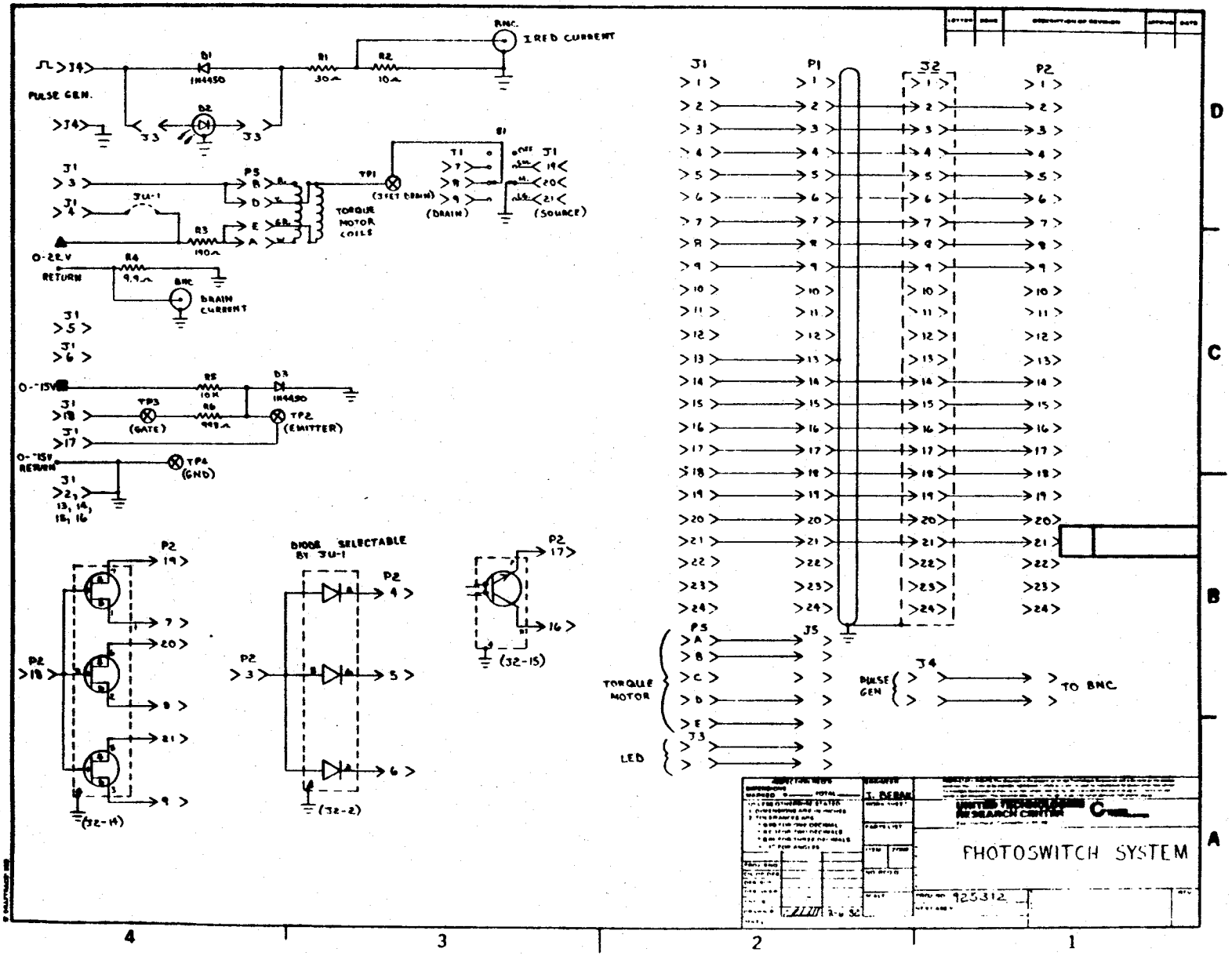


TABLE A-I

PHOTOSWITCH BREADBOARD ELECTRICAL PARTS

R1	30-ohm IRED load resistor
R2	10-ohm IRED current-monitoring resistor
R3	190-ohm Torque-motor load resistor
R4	9.9-ohm Drain-current-monitoring resistor
R5	10K-ohm Gate resistor
R6	998-ohm Gate-current-monitoring resistor
D1	1N4450 Reverse-bias protection diode for D2
D2	Hitachi HLP-50 IRED (λ = 8360Å)
D3	1N4450 Phototransistor protection diode
S1	Rotary switch for JFET selection
J1	Female chassis connector
P1	Male cable connector
J2	Female cable connector
P2	Male connector on high-temperature probe assembly
J3	Teflon socket for IRED
J4	Cable end from pulse generator
J5	Female connector mounted to the torque-motor housing
P5	Male cable connector to torque motor
JU-1	Jumper to select diodes in TO-5 package
	Torque Motor Coils - 32 ohms each coil

TABLE A-II

J1 PIN DESIGNATIONS ON PHOTOSWITCH BREADBOARD

Pin	Function
1	----
2	Ground for diode TO-5 package
3	GaAs diode substrate (common cathode)
4	GaAs 5-mil diameter diode (anode)
5	GaAs 7.5-mil diameter diode (anode)
6	GaAs 10-mil diameter diode (anode)
7	GaAs JFET drain (small device)
8	GaAs JFET drain (medium device)
9	GaAs JFET drain (large device)
10	----
11	----
12	----
13	Ground for wire braid and high-temperature probe assembly
14	Ground for JFET TO-5 package
15	Ground for phototransistor assembly
16	GaAlAs/GaAs phototransistor collector
17	GaAsAs/GaAs phototransistor emitter
18	GaAs JFET substrate gate (common cathode)
19	GaAs JFET source (small device)
20	GaAs JFET source (medium device)
21	GaAs JFET source (large device)
22	----
23	----
24	----

Figure A-4 shows the configuration of breadboard devices used for demonstration of optical switching. Current through the torque motor was controlled by switching the voltage on the JFET gate. A negative gate pinch-off voltage of -12 to -13V was required for the supplied JFETs to switch off drain current; a near-zero voltage turned the JFET into the on-state. The off-state resistances at 250°C for the phototransistor and JFET were used to determine the value of R5 (R5 = 10K) so that at 250°C all but a maximum of 1 volt of the gate power supply voltage could appear at the JFET gate and emitter of the phototransistor. This corresponded to a maximum of 100 μA of offstate current that could flow principally through the JFET gate. If off-state currents were to increase, then R5 would have to decrease to maintain a proper off-state power supply voltage at the JFET gate. When the photo-transistor was illuminated, its resistance decreased and photogenerated current, up to about 1.4 mA, flowed through the phototransistor and R5. With sufficient illumination, the emitter voltage dropped below -0.5V as the photo-transistor resistance became much lower than R5. This pulled the JFET gate to the same voltage value and turned the JFET switch on. From this discussion, it follows that the higher the value of R5 that can be used, then the lower the optical power requirements at the phototransistor. The one-volt drop across R5 was arbitrarily set and represents the maximum JFET gate overdrive for lower-temperature operation.

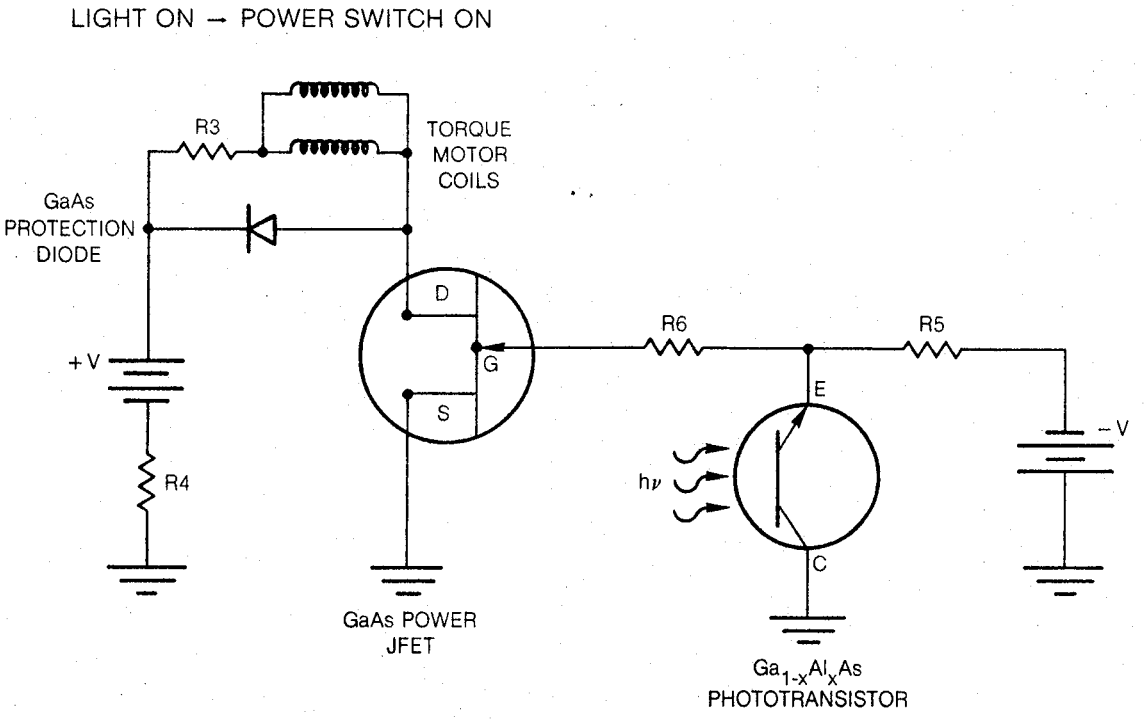
In order to protect the JFET drain when current was switched off to the inductive load, a GaAs transient-protection diode was placed across the torque-motor coils and R3. R3 was added to demonstrate the voltage capability of the photoswitch system. Not shown in Fig. A-4 but included in Fig. A-3 and on the breadboard was an optional silicon diode, D3, which was placed across the phototransistor terminals at the breadboard to protect against positive voltage transients at the emitter terminal. Positive voltage at E will damage the phototransistor. The drain current was obtained by measuring the voltage across R4; JFET gate current was obtained by a differential high-impedance voltage measurement across R6.

7. Torque-Motor Subassembly in Housing

Actually, this part was a torque-motor projector-jet feedback spring subassembly used in Abex valves. The coils were wired in parallel to give an overall 16 ohms dc resistance. These coils were rated at 40 mA each or 80 mA total. Since there was no restoring force on the spring, one was artifically provided by placing an iron slab at the base of the coils. The position of the slab could be adjusted with respect to the coils to control the oscillation. Breadboard photoswitch testing was carried out at a coupling level so that wand oscillation was visible through the cylindrical lens without being driven against internal electromagnet stops.

FIG. A-4

CONFIGURATION OF BREADBOARD DEVICES FOR OPTICAL SWITCHING



83–3–119–33

8. Three Sets of GaAs High-Temperature Devices

A device set for demonstrating photoswitching into inductive loads consisted of a photosensitive element (GaAlAs/GaAs phototransistor), the power device (GaAs JFET) and a GaAs transient-protection diode to protect the drain of the JFET device. One device set was shown in Fig. 4-6. The GaAs JFET and diode were sealed into TO-5 packages. The phototransistor was mounted on a TO-5 base which was sealed to a stainless steel cap assembly having an internal, metallized, fiber-to-tube, hermetic seal. The end of the fiber was positioned just above the photosensitive area of the phototransistor. Fiber protection tubes extended away from the cap to the room-temperature end where the f-o pigtail was internally sealed to the tube with epoxy. A chromel-alumel thermocouple was also spot welded to the phototransistor TO-5 base. The photoswitch system was fully qualified for operation between -55°C and 254°C.

In each TO-5 package for the GaAs transient-protection diode and JFET, there were three possible devices, referred to as small, medium, and large (size). In the case of the diode, the device that was tested on the breadboard was the small diode (115-μm mesa diameter), which had been set by jumper JV-1 (see Fig. A-3). In the case of each of the three JFET packages, only the small JFET device was usable; the medium and large JFET's were either not wired or not functional. There was a JFET selector switch on the front panel of the breadboard which had to be set to S (small) to connect the proper JFET leads to the breadboard circuitry.

9. Photoswitch Probe Assembly

Figure A-5 shows the probe assembly including mounted photoswitch devices. The phototransistor assembly sat inside a slot on the probe. The thermocouple leads ran out along the fiber protection tubes. A brass clamp (not shown) held the tube and probe at a position just before the shrink tubing on the outer protection tube. A stainless-steel cover tube locked onto the probe over the devices. The probe was designed so that the cover tube would fit inside a temperature-controlled environmental chamber, oven or low-temperature dewar. An opening with a diameter of at least 2.9 cm was required for the probe. Only the cover tube and a small length of the larger-diameter stainless-steel protection tube were to be heated or cooled. The aim was to keep the epoxy-fiber-seal area at the brass clamp to as near room temperature as possible.

PHOTOSWITCH PROBE ASSEMBLY

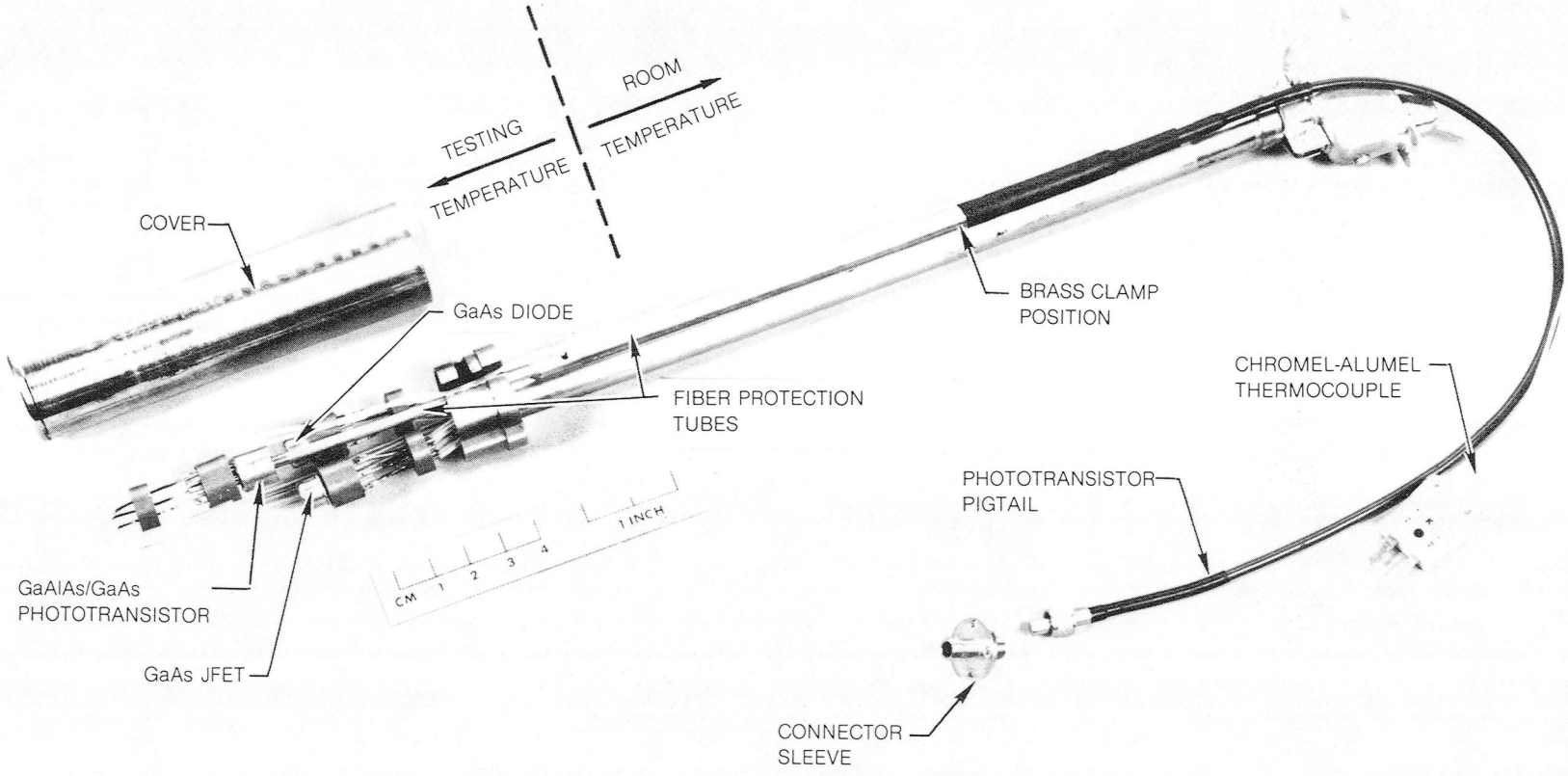


FIG. A-5

APPENDIX II

LIST OF SYMBOLS

A	ampere(s)
Å	angstrom(s)
a_j	JFET junction area
AM	air mass
a_p	photovoltaic area
C	phototransistor collector current
cw	continuous wave operation
D	JFET drain contact
d	diameter
dB	decibel(s)
dc	direct current
d_c	fiber core diameter
d_{max}	diameter of base of light core, 100 μm away from fiber end
d_t	fiber diameter, core plus cladding
E	phototransistor emitter contact
E_{av}	average energy of incident photons
E→E	electrical-to-electrical conversion
E→O	electrical-to-optical conversion
F	optical fiber with core diameter of 1000 μm

f	optical fiber with core diameter of 200 μm
FET	field-effect transistor
FF	photovoltaic fill factor
f-o	fiber optic
G	JFET gate contact
g	phototransistor optical gain
h	Planck's constant
I	electrical current
I_D	JFET drain current
I_d	defect current at heterojunction
I_{Dsat}	JFET saturation drain current
I_E	emitter phototransistor current
I_G	JFET gate current
I_i	phototransistor emitter-base injected current
ILD	injection laser diode
I_{mp}	photovoltaic maximum-power voltage
I_P	phototransistor photocurrent
IRED	infrared-emitting diode
I_{sc}	photovoltaic short-circuit current
I-V	current-voltage
I^2R	power dissipation through resistor
JFET	junction field-effect transistor

J_{mp}	photovoltaic maximum-power current density
J_{sc}	photovoltaic short-circuit current density
K	thermal conductivity
k	Boltzmann's constant
K_s	dielectric constant
L	diffusion length of minority carrier
ℓ	semiconductor absorption depth
L_{coils}	inductance of torque-motor coils
LD	laser diode
ℓ_s	distance through substrate to infinite heat sink
N	GaAlAs electron carrier concentration
n	GaAs electron carrier concentration
n^+	GaAs electron carrier concentration (degenerate)
NA	numerical aperture of optical fiber
n_f	diode ideality factor
N_{ph}	number of photons incident on photovoltaic
$n_{ph}(E_g)$	incident number of photons/second/area of p-n junction with sufficient energy to generate electron-hole pairs
P	GaAlAs hole carrier concentration
p	GaAs hole carrier concentration
p^+	GaAs hole carrier concentration (degenerate)

PCE	photovoltaic power-conversion efficiency
P_d	electrical power dissipation in diode
P_o	optical power incident on photodevice
PR	photoresist
PT	phototransistor
PV	photovoltaic
Q	fraction of photogenerated carriers collected in photovoltaic
q	charge of current carrier
r	reflection coefficient
R_{coils}	resistance of torque-motor coils
r_d	radius of protection diode
r_f	resistance factor for photovoltaic cell
R_G	JFET gate resistance (dc) to source
R_{mp}	photovoltaic maximum-power load resistance (dc)
R_p	resistor in Case-I photoswitch circuit
R_S	photovoltaic internal series resistance (ohm-cm^2)
R_s	resistor in Case-II photoswitch circuit
S	JFET source contact
sec	second(s)
T	temperature

t	thickness
t_b	thickness of phototransistor base layer
t_c	thickness of n-type material in channel of JFET
t_D	thickness of n-type material under drain of JFET
t_d	depletion thickness of p^+-n junction
UTRC	United Technologies Research Center
V	volt(s)
V_B	diode breakdown voltage
V_b	built-in voltage of p-n junction
V_D	JFET drain voltage
V_G	JFET gate voltage
VMIS	vertical metal-insulator-semiconductor (device)
VMOS	vertical metal-oxide-semiconductor (device)
V_{mp}	photovoltaic maximum-power voltage
V_{oc}	photovoltaic open-circuit voltage
V_p	JFET pinch-off voltage
W	watt(s)
x	atom fraction of Al in $Ga_{1-x}Al_xAs$
X_2	halogen
Z	JFET gate width

α	absorption coefficient for light in semiconductor
β	transistor common-emitter current gain
ε_o	permittivity of free space
Λ	$\sim q/kT$
λ	wavelength
η	ratio of photovoltaic electrical power output to optical power arriving per unit area
ν	frequency
Ω	ohm(s)

Delivered High-Temperature Photoswitch Devices

O13a	GaAlAs/GaAs phototransistor
K11d	GaAlAs/GaAs phototransistor
R14a	GaAlAs/GaAs phototransistor
D7s	GaAs JFET
M8s	GaAs JFET
H6s	GaAs JFET
D1s	GaAs transient-protection diode
D2s	GaAs transient-protection diode
D3s	GaAs transient-protection diode

See Table A-I for symbols used in the breadboard circuit diagram (Fig. A-3).

REFERENCES

1. Sze, S. M., "Physics of Semiconductor Devices", Second Edition (John Wiley and Sons, N.Y., 1981), Chapter 1.

2. Kamath, S., Knechtli, R. C., Schwartz, S., and Wolff, G., "GaAs Concentrator Photovoltaic Power System Feasibility Investigation", AFAPL-TR-76-C-2142, Air Force Aero Propulsion Laboratories, Hughes Aircraft Company, September 1977.

3. Grove, A. S., "Physics and Technology of Semiconductor Device" (John Wiley and Sons, N.Y., 1967), Chapter 2.

4. Kroemer, H., "Theory of a Wide-Gap Emitter for Transistors", Proc. Inst. Radio Eng. 45, 1535-7 (1957).

5. Konagai, M., and Takahashi, K., "(GaAl)As-GaAs Heterojunction Transistors with High Injection Efficiency", J. Appl. Phys. 46, 2120-4 (1975).

6. Milano, R. A., Windhorn, T. W., Anderson, E. R., Stillman, G. E., Dupuis, R. D., and Dapkus, P. D., "AlGaAs-GaAs Heterojunction Phototransistors for Fiber-Optical Communications", Proceedings of IEEE International Electron Devices Meeting, Washington, D.C., p. 650-2, December 1978. "$Al_{0.5}$ $Ga_{0.5}As$-GaAs Heterojunction Phototransistors Grown by Metalorganic Chemical Vapor Deposition", App. Phys. Lett. 34, 562-4 (1979).

7. Alferov, Z. I., Akhmedov, F. A., Korol'kov, V. I., and Nikitin, V. G., "Phototransistor Utilizing a GaAs-AlAs Heterojunction", Sov. Phys. Semicond. 7, 780-2 (1973).

8. Konagai, K., Katsukawa, K., and Takahashi, K., "(GaAl)As/GaAs Heterojunction Phototransistors with High Current Gain", J. Appl. Phys. 48, 4389-94 (1977).

9. Beneking, H., Mischel, P., and Schul, G., "High-Gain Wide-Gap-Emitter $Ga_{1-x}Al_xAs$-GaAs Phototransistor", Elect. Lett. 12, 395-6 (1976).

10. Nelson, H., and Kressel, H., "Improved Red and Infrared Light Emitting $Al_xGa_{1-x}As$ Laser Diodes Using the Close-Confinement Structure", Appl. Phys. Lett. 15, 7-9 (1969).

11. Oldham, W., and Milnes, A., "Interface States in Abrupt Semiconductor Heterojunctions", Solid State Electron. 7, 153-65 (1964).

12. Hovel, H. J., and Woodall, J. M., "Theoretical and Experimental Evaluations of $Ga_{1-x}Al_xAs$-GaAs Solar Cells", Conference Record of the 10th IEEE Photovoltaic Specialists Conference, Palo Alto, California, 1973 (IEEE, New York, 1974), p. 25-30.

13. Deitch, R. H., "Liquid-Phase Epitaxial Growth of Gallium Arsenide Under Transient Thermal Conditions", J. Crystal Growth 7, 69-73 (1970).

14. Berak, J. M., Grantham, D. H., and Swindal, J. L., "Gallium Arsenide High-Temperature Electronic Devices", Final Report Contract No. N00019-76-C-0673, NASC, United Technologies Research Center, October 1977.

15. Bailbe, J., Marty, A., Hiep, P., and Rey, G., "Design and Fabrication of High-Speed GaAlAs/GaAs Heterojunction Transistors", IEEE Trans. Electron Devices ED-27, p. 1160-4 (1980).

16. Svilans, M. N., Grote, N., and Beneking, H., "Sensitive GaAlAs/GaAs Wide-Gap Emitter Phototransistor for High-Current Applications", IEEE Electron Device Lett. EDL-1, p. 247-9, 1980.

17. International Newsletter, Electronics, p. 55, January 27, 1982.

18. "Handbook of Fiber Optics: Theory and Applications", edited by H. Wolf, (Garland Press, New York, 1979), p. 79.

19. Wolf, M., "Outlook for Si Photovoltaic Devices for Terrestrial Solar-Energy Utilization", J. Vac. Sci. Technol. 12, 984-99 (1975).

20. Ettenberg, M., and Kressel, H., "Interfacial Recombination at (AlGa)As/GaAs Heterojunction Structures", J. Appl. Phys. 47, 1538-44 (1976).

21. Ewan, J., Knechtli, R. C., Loo, R., and Kamath, G. S., "GaAs Solar Cells for High Solar Concentration Applications", Conference Record of the 13th Photovoltaic Specialists Conference, Washington, D.C., 1978 (IEEE, New York, 1978), p. 941-5.

22. Vander Plas, H. A., James, L. W., Moon, R. L., and Nelson, N. J., "Performance of AlGaAs/GaAs Terrestrial Concentrator Solar Cells", Conference Record of the 13th Photovoltaic Specialists Conference, Washington, D. C., 1978 (IEEE, New York, 1978), p. 934-40.

23. Sahai, R., Edwall, D. D., and Harris, Jr. J. S., (a) "High Efficiency AlGaAs/GaAs Concentrator Solar Cell Development", Conference Record of the 13th Photovoltaic Specialists Conference, Washington, D.C., 1978 (IEEE, New York, 1978), p. 946-52. (b) "High Efficiency AlGaAs/GaAs Concentrator Solar Cells", Appl. Phys. Lett. 34, 147-9 (1979).

24. Charan, S., Konagai, M., and Takahashi, K., "Series Resistance Effects in (GaAl)As/GaAs Concentrator Solar Cells", J. Appl. Phys. 50, p. 963-8 (1979).

25. James, L. W., and Moon, R. L., "GaAs Concentrator Solar Cell", Appl. Phys. Lett. 26, 467-70 (1975).

26. Turner, G. W., Fan, J. C. C., Chapman, R. L., and Gale, R. P., "GaAs Shallow Homojunction Concentrator Solar Cells", Conference Record of the 15th Photovoltaic Specialists Conference, Kissimmee, Florida, 1981 (IEEE, New York, 1981), p. 151-5.

27. Curtis, H. B., "Determination of Optimum Sunlight Concentration Level in Space for GaAs Solar Cells", Conference Record of the 15th Photovoltaic Specialists Conference, p. 52-6.

28. Walker, G. H., and Conway, E. J., "High Temperature Properties of GaAlAs/GaAs Heteroface Solar Cells", Conference Record of the 14th Photovoltaic Specialists Conference, San Diego, California, 1980 (IEEE, New York, 1980), p. 1098-1101.

29. Chaffin, R. J., "Thermal Impedance Effects in GaAs High Concentration Photovoltaic Cells", Conference Record of the 15th Photovoltaic Specialists Conference, Kissimmee, Florida (IEEE, New York, 1981), p. 173-7.

30. James, L. W., and Moon, R. L., "GaAs Concentrator Solar Cells", Conference Record of the 11th Photovoltaic Specialistis Conference, Scottsdale, Arizona, 1975 (IEEE, New York, 1975), p. 402-8.

31. O'Donnell, D. T., Robb, S. P., Rule, T. T., Sanderson, R. W., and Backus, C. E., "Performance of Silicon and Gallium Arsenide Concentration Cells", Conference Record of the 13th Photovoltaic Specialists Conference, Washington, D.C., 1978 (IEEE, New York, 1978), p. 804-9.

32. Temkin, H. and Keramides, V. G., Room Temperature Conductivity and the Band Structure of n-$Ga_{1-x}Al_xAs$", J. Appl. Phys. 51, 3269-72 (1980).

33. SpringThorpe, A. J., King, F. D., and Becke, A., "Te and Ge - Doping Studies in $Ga_{1-x}Al_xAs$", J. Electronic Mater. 4, 101-18 (1975).

34. Green, M. A., "General Solar Cell Curve Factors Including the Effects of Ideality Factor, Temperature and Series Resistance", Solid-St. Electron 20, 265-6 (1977).

35. Loferski, J. J., "Theoretical Considerations Governing the Choice of the Optimum Semiconductor for Photovoltaic Solar Energy Conversion", J. Appl. Phys. 27, 96 (1956).

36. Rasmussen, N. E., and Branz, H. M., "The Dependence of Delivered Energy on Power Conditioner Electrical Characteristics for Utility Interactive PV Systems", Op. Cit., 15th Photovoltaic Specialists Conference, p. 614-620.

37. Private Communication, Landsman, M., and Lyons, W., American Power Conversion Corp., Burlington, Mass.

38. Santic, A., and Neuman, M. R., "A Low Voltage dc-dc Converter for Implanted Electronic Circuits", J. Bioengineering 1, 357-68 (1977).

39. Robertson, M. M., "Power Transfer via Fiber Optics", Confrence Record of the 12th Photovoltaic Specialists Conference, Baton Rouge, Louisiana, 1976 (IEEE, New York, 1977), p. 216-220.